



Features

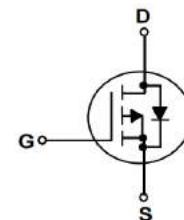
- P-Channel
- High density celldesign for ultra low on-resistance
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- 100% EAS Tested

V_{DS}	-100	V
$R_{DS(on),TYP}$ @ $V_{GS}=-10$ V	120	mΩ
$R_{DS(on),TYP}$ @ $V_{GS}=-4.5$ V	122	mΩ
I_D	-15	A

TO-252



Part ID	Package Type	Marking	Packing
ZT120P10D	TO-252	ZT120P10D	2500pcs/reel



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_c=25^\circ\text{C}$ Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	± 20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	-100	V	
T_J	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature Range	-55 to 150	°C	
I_{DM}	Drain Current-Continuous@ Current-Pulsed	$T_c=25^\circ\text{C}$	-52	A
Mounted on Large Heat Sink				
I_D	Drain Current-Continuous	$T_c=25^\circ\text{C}$	-15	A
		$T_c=100^\circ\text{C}$	-9.2	A
P_D	Maximum Power Dissipation	$T_c=25^\circ\text{C}$	40	W
	Derating factor		0.27	W/°C
$R_{\theta JC}$	Thermal Resistance-Junction to Case (Note 2)	3.75	°C/W	
Drain-Source Avalanche Ratings				
EAS	Avalanche Energy, Single Pulsed (Note 5)	110	mJ	



Electrical Characteristics ($T_j=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-100	--	--	V
Idss	Zero Gate Voltage Drain Current	$V_{DS}=-100\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.4	-1.7	-2.5	V
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=-10\text{V}, I_D=-15\text{A}$	--	120	150	$\text{m}\Omega$
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=-4.5\text{V}, I_D=-10\text{A}$	--	122	180	$\text{m}\Omega$
gFS	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-5\text{A}$	12	--	--	S

Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated) ^(Note 4)

Ciss	Input Capacitance	$V_{DS}=-50\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	--	1732	--	pF
Coss	Output Capacitance		--	85	--	pF
Crss	Reverse Transfer Capacitance		--	40	--	pF
Qg	Total Gate Charge	$V_{DS}=-50\text{V}, I_D=-10\text{A}, V_{GS}=-10\text{V}$	--	33	--	nC
Qgs	Gate-Source Charge		--	4.2	--	nC
Qgd	Gate-Drain Charge		--	7.1	--	nC

Switching Characteristics ^(Note 4)

Td(on)	Turn-on Delay Time	$V_{DS}=-50\text{V}, I_D=-10\text{A}, R_G=9.1\Omega, V_{GS}=-10\text{V}$	--	12	--	ns
Tr	Turn-on Rise Time		--	52	--	ns
Td(off)	Turn-Off Delay Time		--	28	--	ns
Tf	Turn-Off Fall Time		--	38	--	ns

Source-Drain Diode Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

ISD	Source-Drain Current (Body Diode) ^(Note 2)		--	--	-15	A
VSD	Forward on voltage ^(Note 3)	$I_S = -10\text{A}, V_{GS}=0\text{V}$	--	--	-1.4	V
Trr	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_F = -10\text{A}, V_{GS}=0\text{V}$ $dI/dt = 100\text{A}/\mu\text{s}$	--	35	--	ns
Qrr	Reverse Recovery Charge		--	46	--	nC

Notes:

- Repetitive Rating: Pulse width limited by maximum junction temperature.
- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production
- E_{AS} condition: $T_j=25^\circ\text{C}, V_{DD}=-50\text{V}, V_G=-10\text{V}, L=0.5\text{mH}, R_g=25\Omega$



Typical Electrical and Thermal Characteristics (Curves)

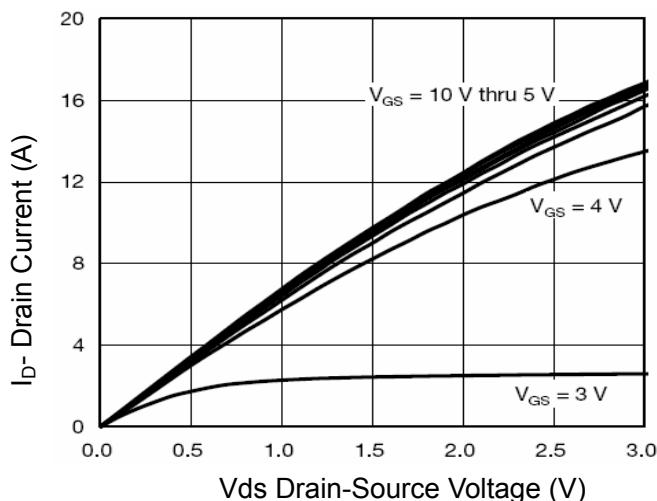


Figure 1 Output Characteristics

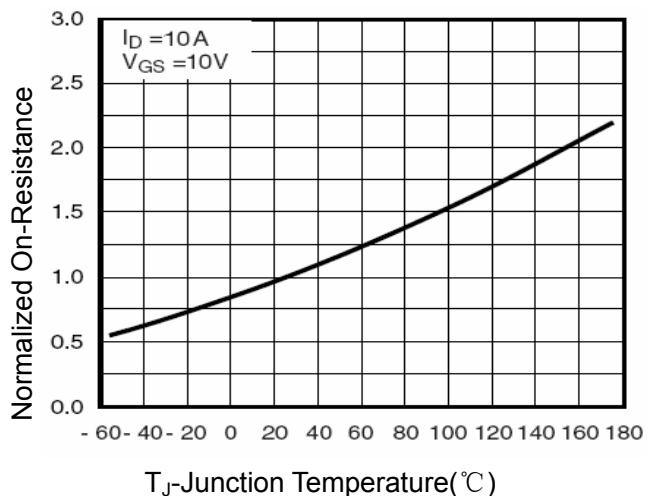


Figure 4 Rdson-JunctionTemperature

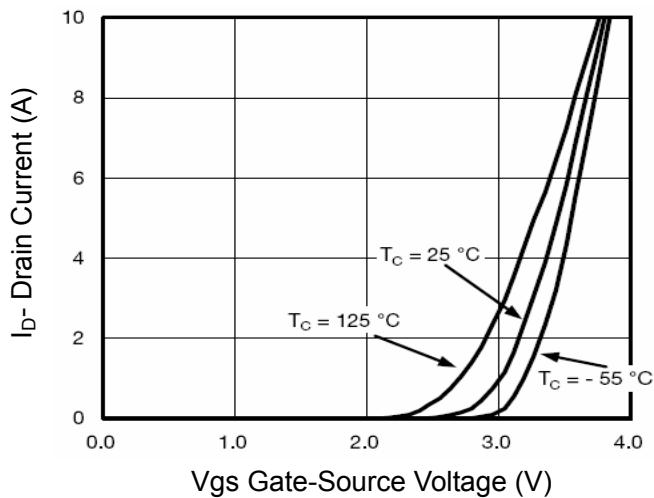


Figure 2 Transfer Characteristics

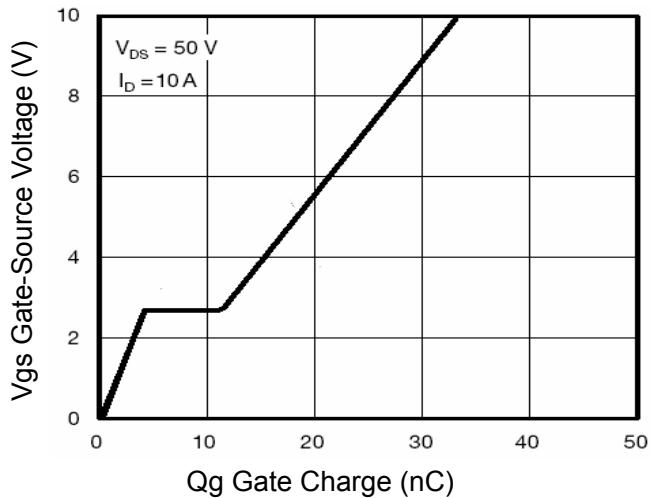


Figure 5 Gate Charge

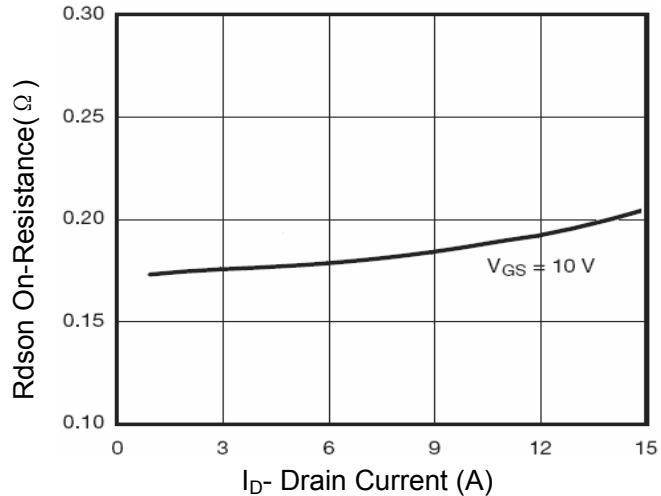


Figure 3 Rdson- Drain Current

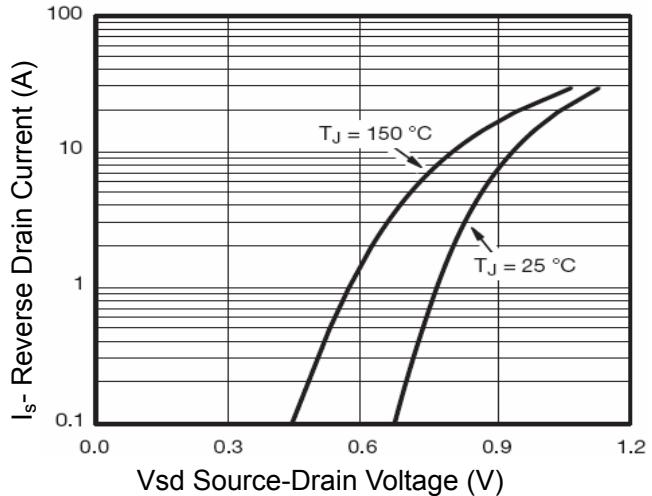


Figure 6 Source- Drain Diode Forward

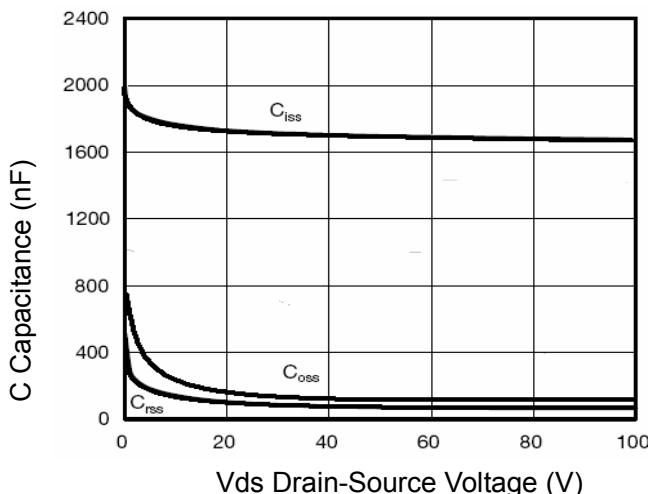


Figure 7 Capacitance vs Vds

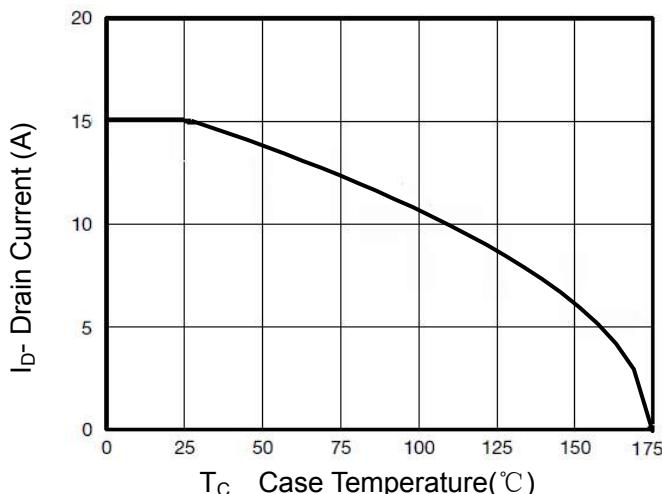


Figure 9 Drain Current vs Case Temperature

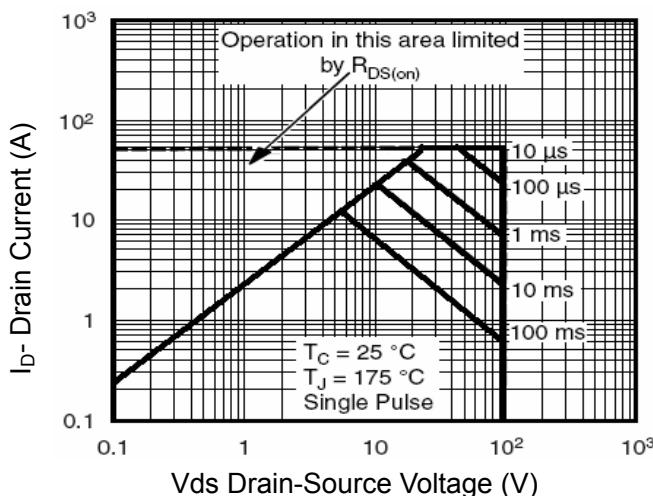


Figure 8 Safe Operation Area

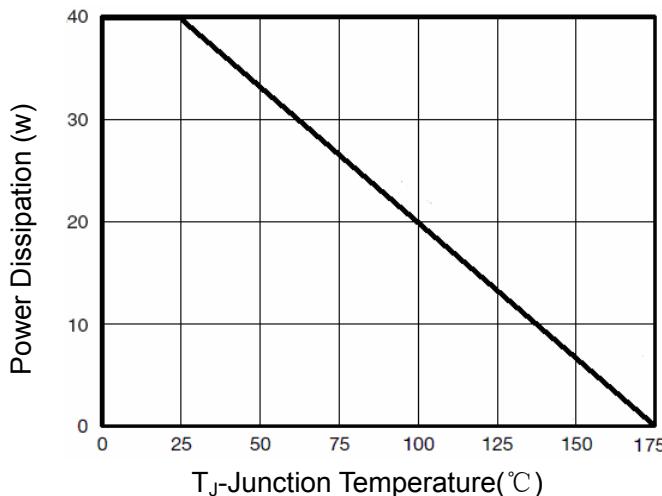


Figure 10 Power De-rating

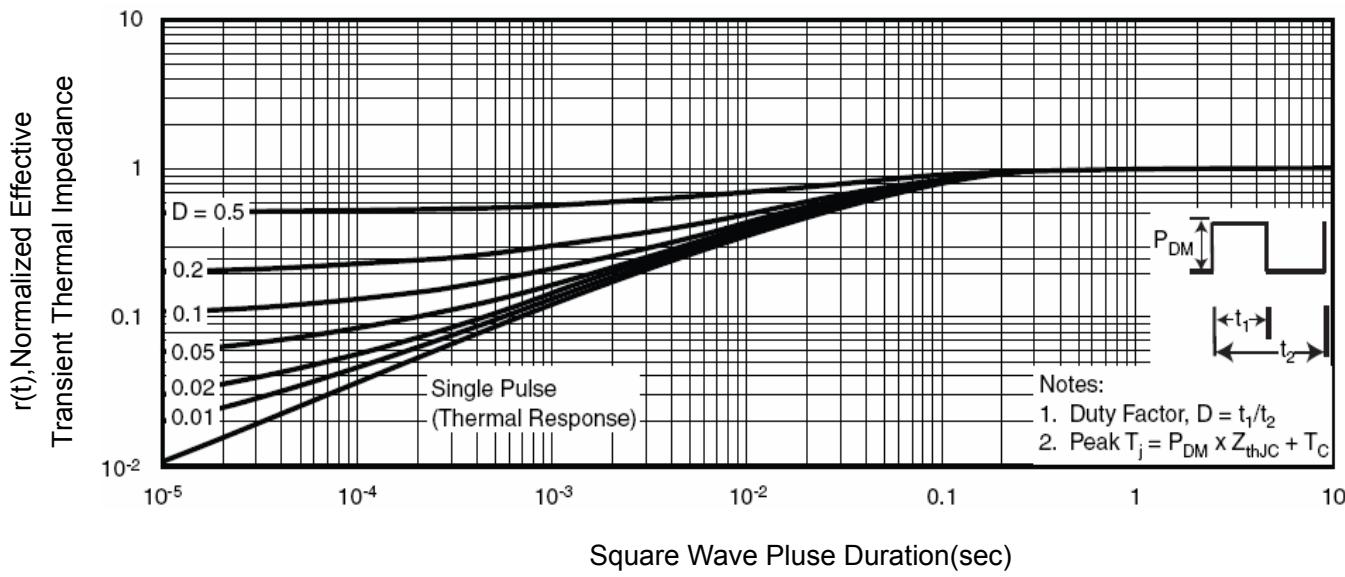
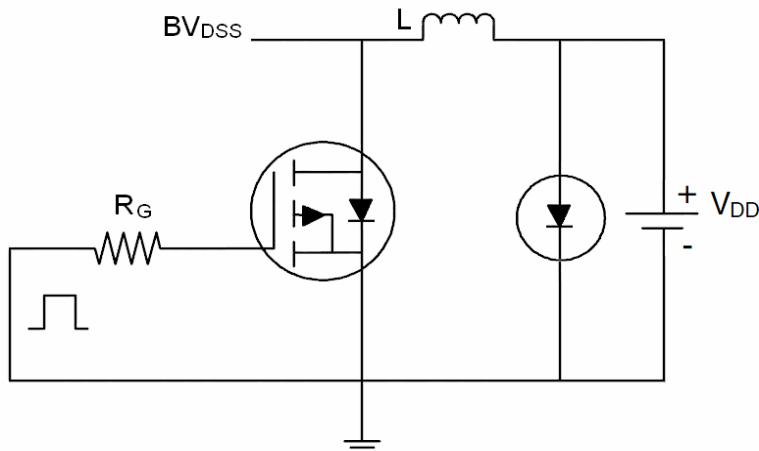


Figure 11 Normalized Maximum Transient Thermal Impedance

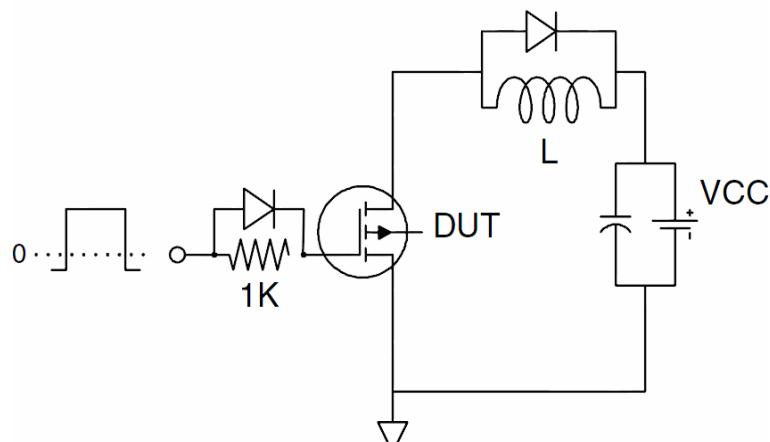


Test Circuit

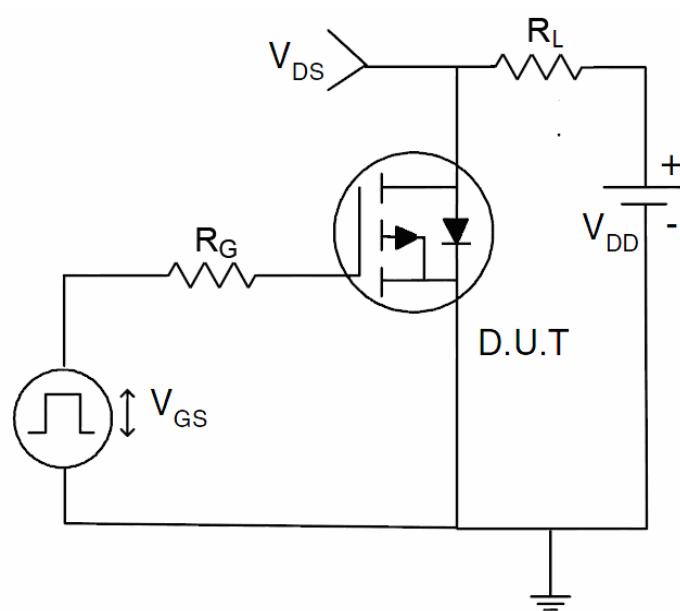
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit

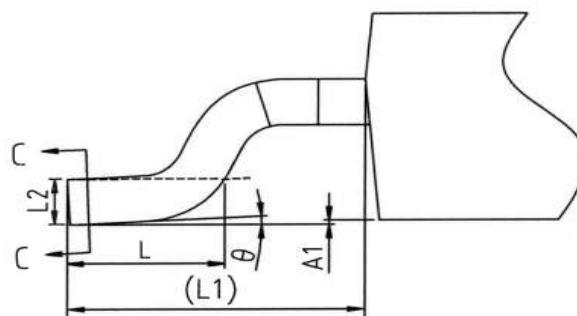
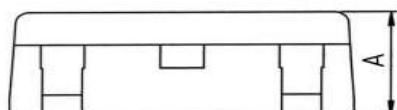
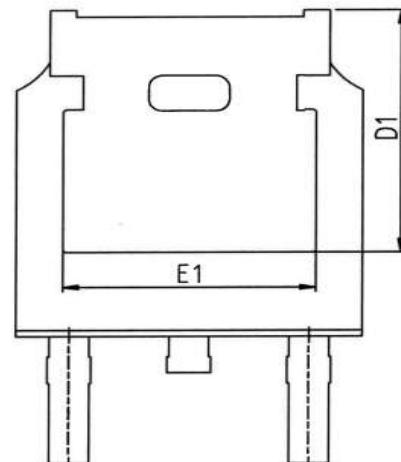
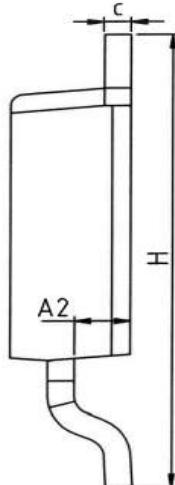
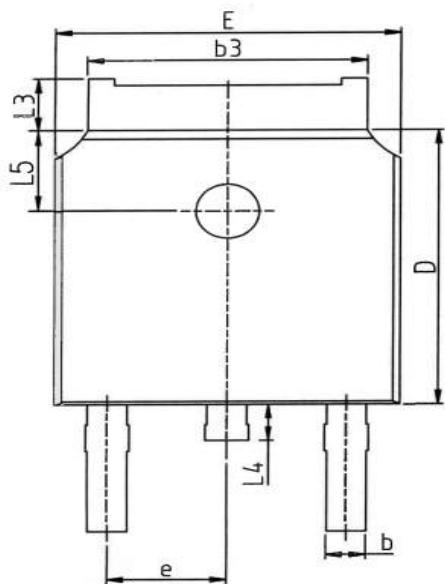


3) Switch Time Test Circuit





TO-252 Package Information



SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°

Customer Service

Sales and Service:

zj@ztasemi.com