

Features

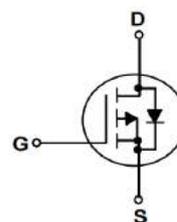
- P-Channel
- Green Device Available
- Low Gate Charge
- Advanced High Cell Density Trench Technology
- 100% EAS Tested

V_{DS}	-30	V
$R_{DS(on),TYP@ V_{GS}=-10V}$	3.5	m Ω
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	4.8	m Ω
I_D	-90	A

DNF5x6



Part ID	Package Type	Marking	Packing
ZT035P03G	DNF5x6	ZT035P03G	5000pcs/reel



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	± 20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	-30	V	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
I_{DM}	Drain Current-Continuous@ Current-Pulsed (Note 1)	$T_C = 25^\circ\text{C}$ -360	A	
Mounted on Large Heat Sink				
I_D	Drain Current-Continuous	$T_C = 25^\circ\text{C}$	-90	A
		$T_C = 100^\circ\text{C}$	-57	A
P_D	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	60	W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		2.08	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient (Note 3)		55	$^\circ\text{C/W}$
Drain-Source Avalanche Ratings				
EAS	Avalanche Energy, Single Pulsed (Note 2)		125	mJ

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V	--	--	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Drain-Source On-State Resistance (Note 4)	V _{GS} =-10V, I _D =-30A	--	3.5	4.5	mΩ
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-4.5V, I _D =-15A	--	4.8	6.2	mΩ
g _{FS}	Forward Transconductance (Note 4)	V _{DS} =-10V, I _D =-30A	--	90	--	S
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	--	5065	--	pF
C _{oss}	Output Capacitance		--	694	--	pF
C _{rss}	Reverse Transfer Capacitance		--	579	--	pF
R _g	Gate Resistance	f=1MHz	--	4.0	--	Ω
Q _g	Total Gate Charge	V _{DS} =-15V, I _D =-30A, V _{GS} =-10V	--	145	--	nC
Q _{gs}	Gate-Source Charge		--	21.3	--	nC
Q _{gd}	Gate-Drain Charge		--	38	--	nC
Switching Characteristics (Note 5)						
T _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, I _D =-30A, R _G =3Ω, V _{GS} =-10V	--	21	--	ns
T _r	Turn-on Rise Time		--	15	--	ns
T _{d(off)}	Turn-Off Delay Time		--	128	--	ns
T _f	Turn-Off Fall Time		--	28	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
I _{SD}	Source-Drain Current (Body Diode)		--	--	-90	A
V _{SD}	Forward on voltage (Note 4)	I _S =-30A, V _{GS} =0V	--	--	-1.2	V

Note :

1. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -50A
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristics

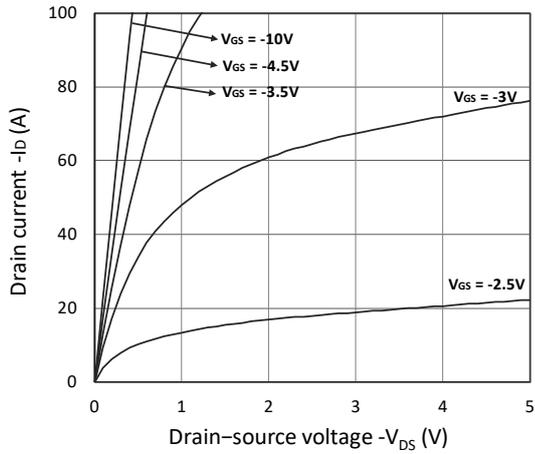


Figure 1. Output Characteristics

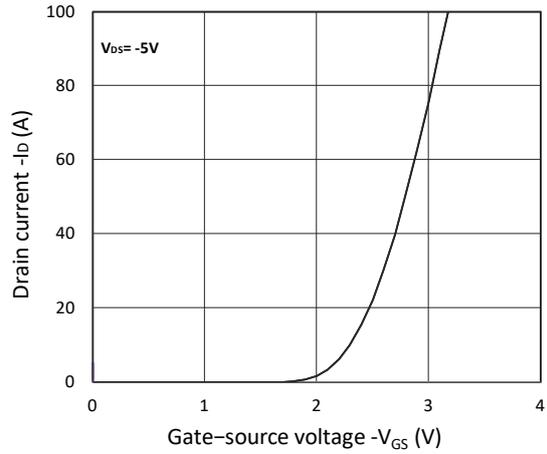


Figure 4. Transfer Characteristics

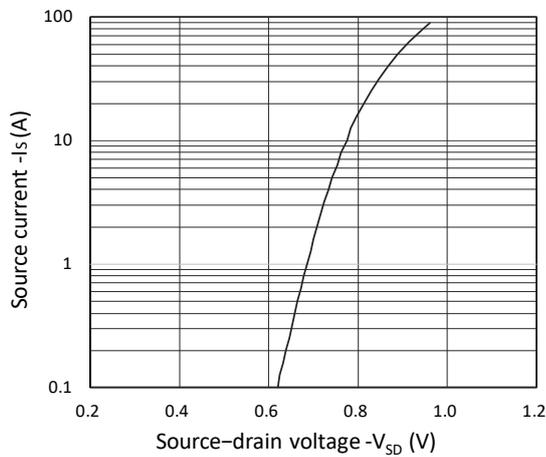


Figure 2. Forward Characteristics of Reverse

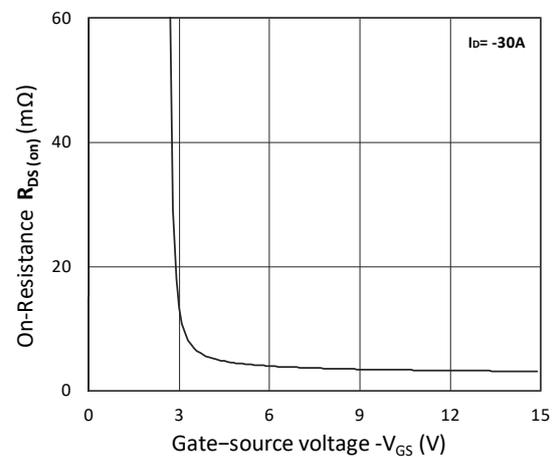


Figure 5. $R_{DS(ON)}$ vs. V_{GS}

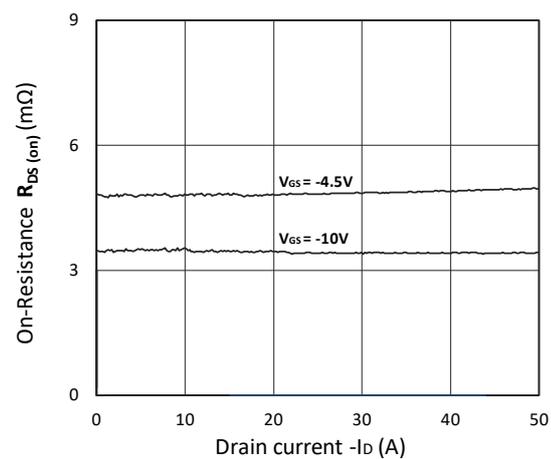


Figure 3. $R_{DS(ON)}$ vs. I_D

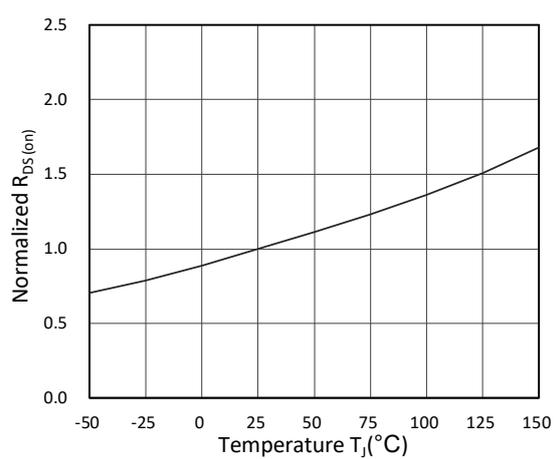


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

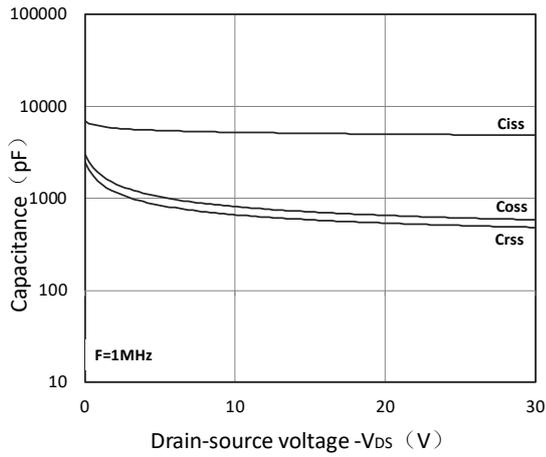


Figure 7. Capacitance Characteristics

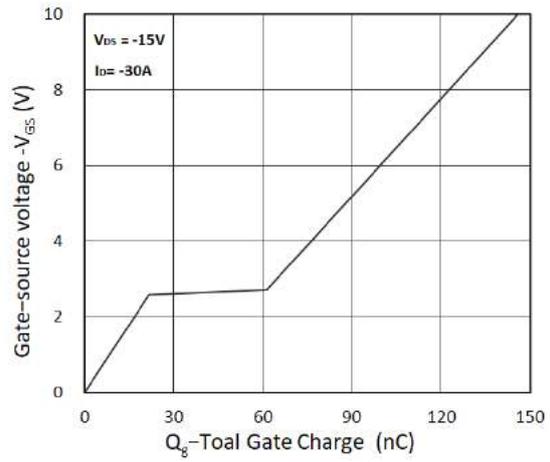


Figure 9. Gate Charge Characteristics

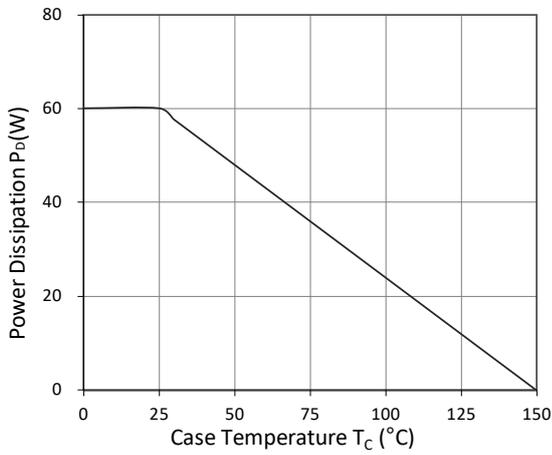


Figure 8. Power Dissipation

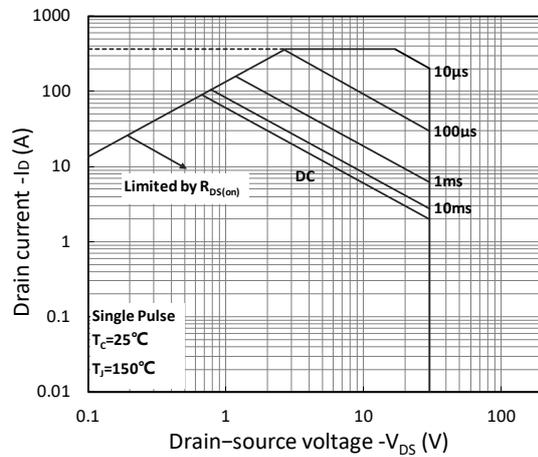


Figure 10. Safe Operating Area

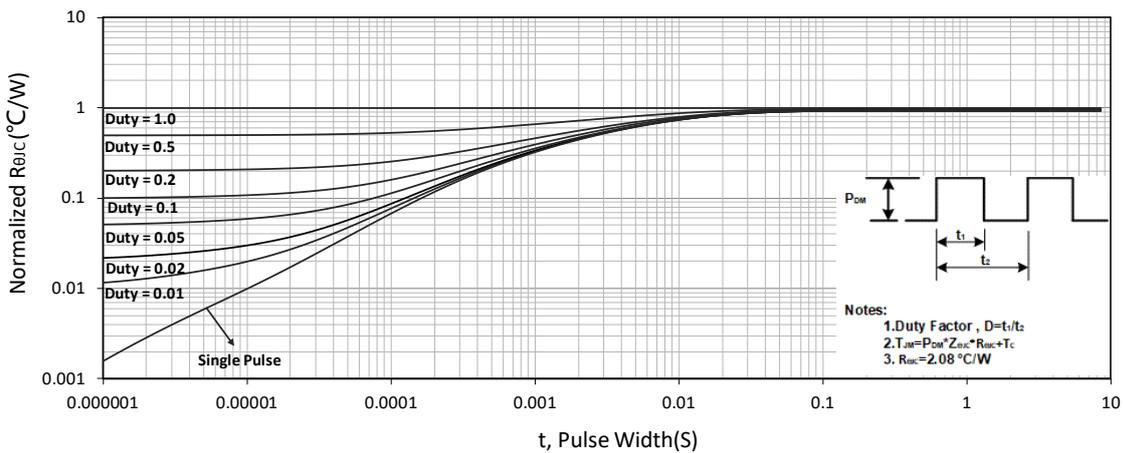
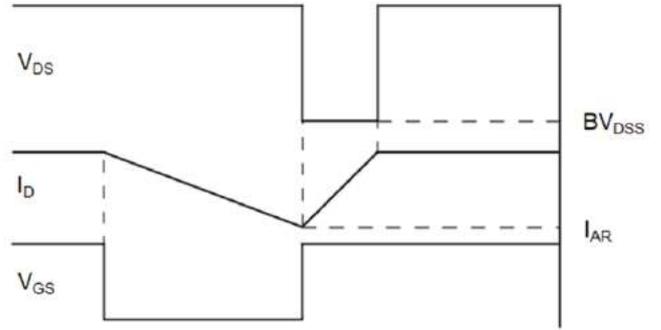
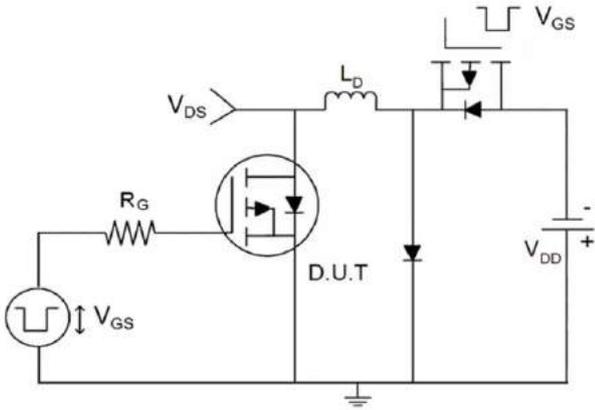


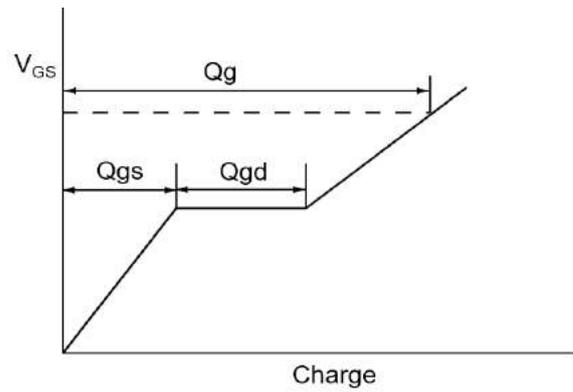
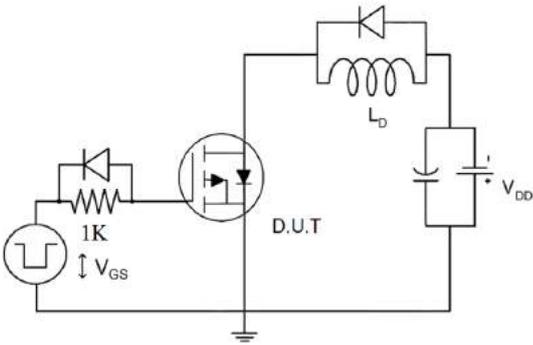
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

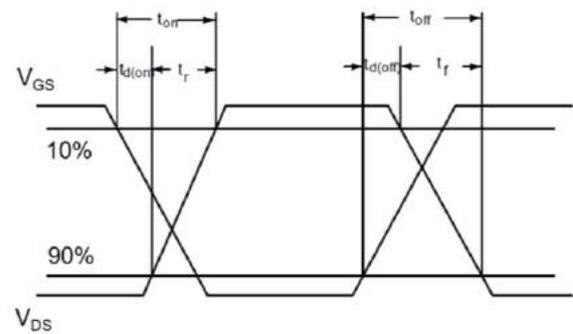
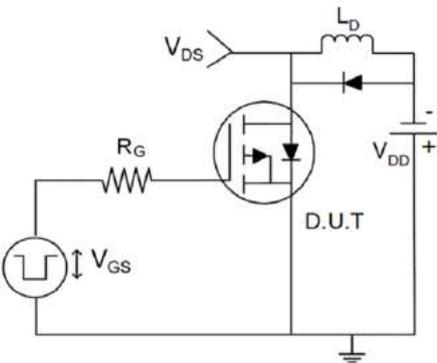
1) E_{AS} Test Circuits



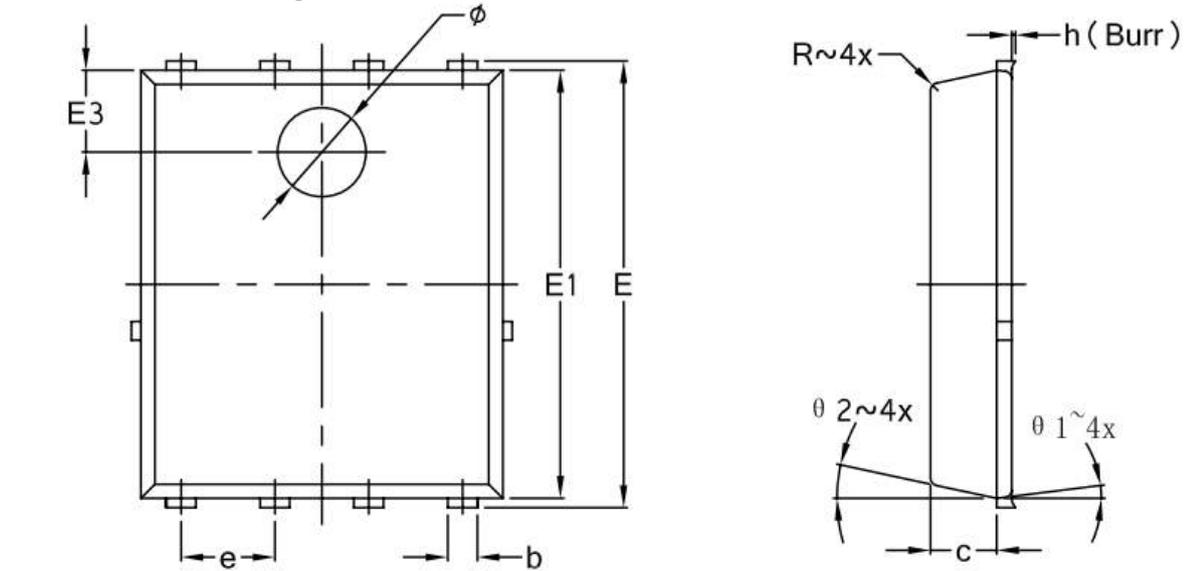
2) Gate Charge Test Circuit



3) Switch Time Test Circuit



DFN5x6-8L Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.35	0.46	0.0138	0.0181
c	0.84	0.95	0.0331	0.0374
D	4.83	5.37	0.1902	0.2114
D1	4.14	4.28	0.1630	0.1685
D2	4.83	4.97	0.1902	0.1957
E	6.03	6.13	0.2374	0.2413
E1	5.68	5.82	0.2236	0.2291
E2	1.65	—	0.0650	—
E3	1.03	1.17	0.0406	0.0461
e	1.27 BSC		0.0500 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.40	0.48	0.0157	0.0189
L2	0.40	0.48	0.0157	0.0189
H	3.315	3.475	0.1305	0.1368
I	—	0.16	—	0.0063
phi	1.13	1.27	0.0445	0.0500
R	0.10		0.0039	
theta 1	7° REF		7° REF	
theta 2	12° REF		12° REF	
h	0.08 MAX		0.0031	

Customer Service

Sales and Service:

zj@ztasemi.com