

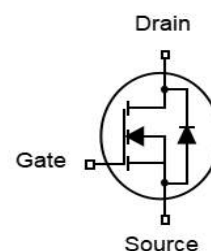
Features

- N-Channel
- Low FOM $R_{DS(ON)} \times Q_G$
- Ultra-low on-resistance
- RoHS compliant ^(Note 1)
- Halogen-free ^(Note 1)
- 100% EAS Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	5.5	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	7.0	mΩ
I_D	50	A

DFN5x6


Part ID	Package Type	Marking	Packing
ZTG055N04G	DFN5x6	ZTG055N04G	5000pcs/Reel



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	±20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V	
T_J	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature Range	-55 to 150	°C	
I_{DM}	Drain Current-Continuous@ Current-Pulsed ^(Note 2)	$T_C = 25^\circ\text{C}$ 200	A	
Mounted on Large Heat Sink				
I_D	Drain Current-Continuous ^(Note 1)	$T_C = 25^\circ\text{C}$	50	A
		$T_C = 100^\circ\text{C}$	32	A
P_D	Maximum Power Dissipation	34	W	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.7	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Steady State ^(Note 4)	49.8	°C/W	
Drain-Source Avalanche Ratings				
EAS	Avalanche Energy, Single Pulsed ^(Note 3)	45.5	mJ	

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.6	2.1	V
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =20A	--	5.5	6.6	mΩ
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =15A	--	7.0	10	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	842	--	pF
C _{oss}	Output Capacitance		--	321	--	pF
C _{rss}	Reverse Transfer Capacitance		--	13	--	pF
R _g	Gate Resistance	f=1MHz	--	4.2	--	Ω
Q _g	Total Gate Charge	V _{DD} =20V, I _D =20A, V _{GS} =10V	--	13.5	--	nC
Q _{gs}	Gate-Source Charge		--	2.4	--	nC
Q _{gd}	Gate-Drain Charge		--	2.6	--	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =20V, R _L =1.0Ω, R _G =1.6Ω, V _{GS} =10V	--	5.5	--	ns
T _r	Turn-on Rise Time		--	49.5	--	ns
T _{d(off)}	Turn-Off Delay Time		--	18	--	ns
T _f	Turn-Off Fall Time		--	5.5	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
I _S	Diode Forward Current		--	50	--	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current ^(Note 1)		--	200	--	A
V _{SD}	Forward on voltage	I _S =20A, V _{GS} =0V	--	--	1.2	V
T _{rr}	Reverse Recovery Time	V _{DD} =20V, I _D =20A di/dt=100A/μs	--	28.6	--	ns
Q _{rr}	Reverse Recovery Charge		--	15	--	nC

Notes:

1. The max drain current rating is package limited
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L = 0.5 mH, V_{DD} = 20V, I_{AS} = 13.5 A, R_G = 25 Ω, Starting T_J = 25 °C
4. Mount on minimum PCB layout

Electrical Characteristics Diagrams

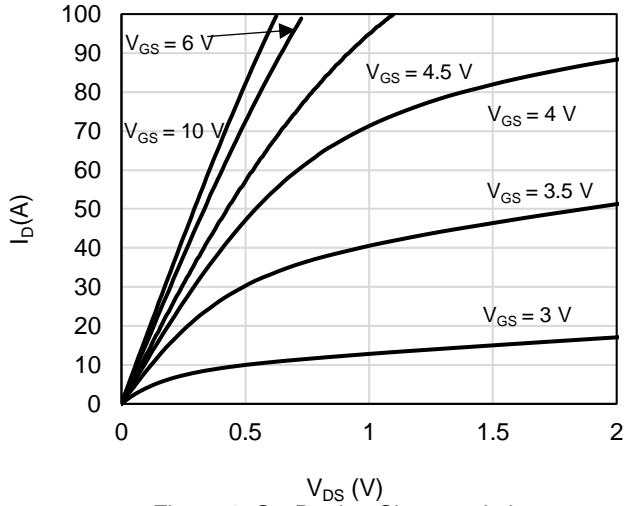


Figure 1: On-Region Characteristics

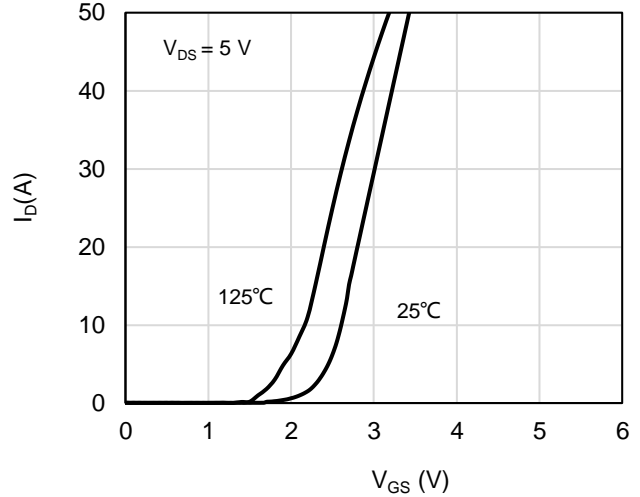


Figure 4: Transfer Characteristics

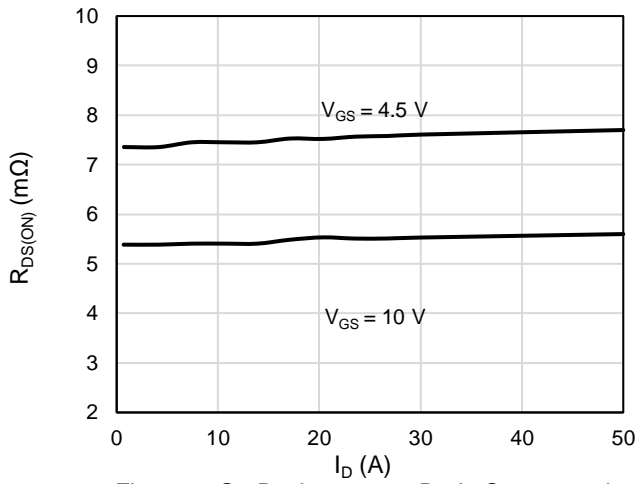


Figure 2: On-Resistance vs. Drain Current and Gate Voltage

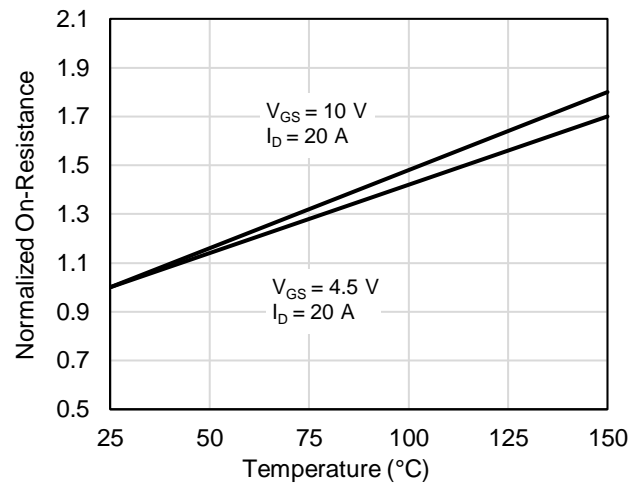


Figure 5: On-Resistance vs. Junction Temperature

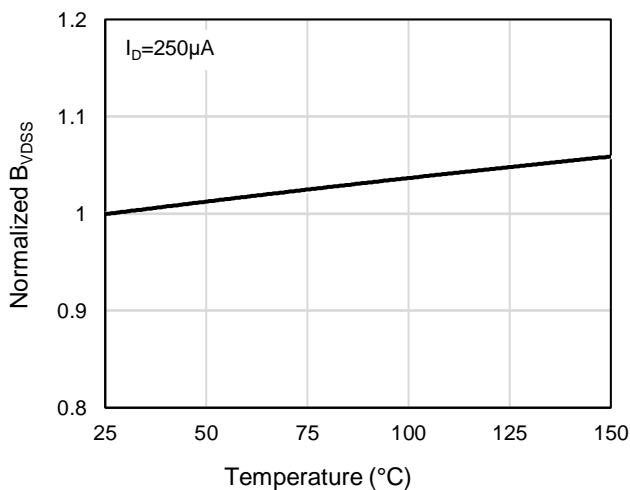


Figure 3: Breakdown Voltage vs. Junction Temperature

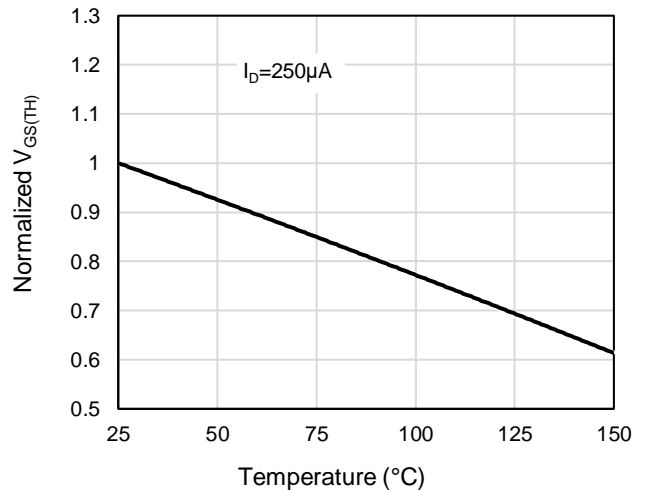


Figure 6: Threshold Voltage vs. Junction Temperature

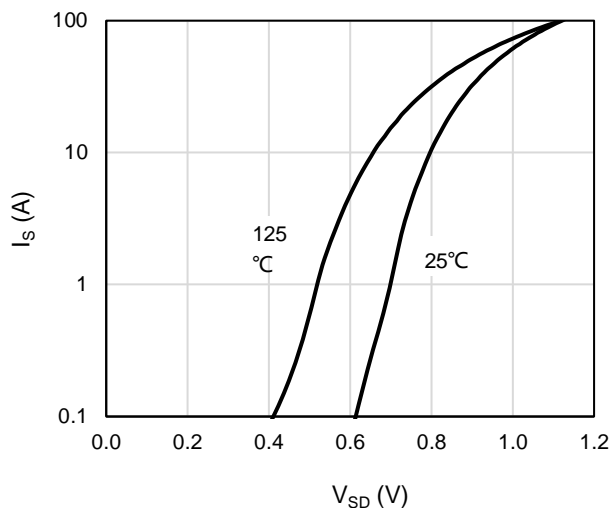


Figure 7: Body-Diode Characteristics

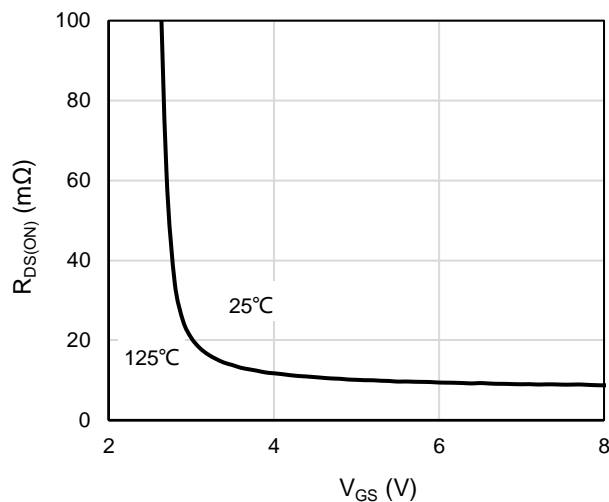


Figure 10: On-Resistance vs. Gate-Source Voltage

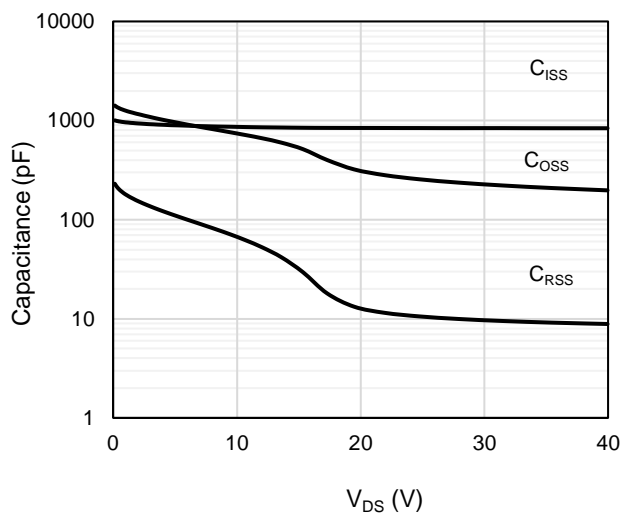


Figure 8: Capacitance Characteristics

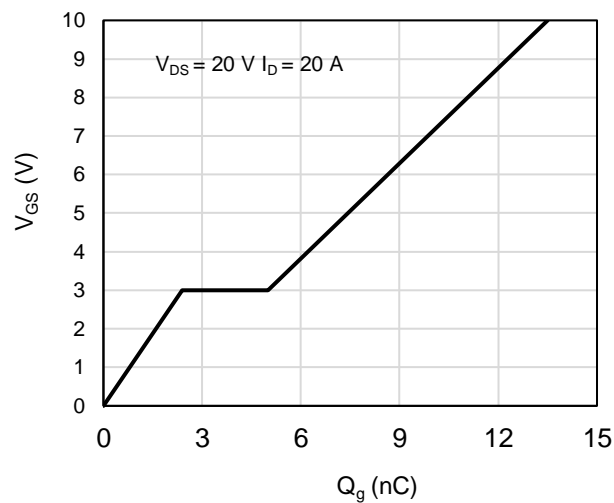


Figure 11: Gate-Charge Characteristics

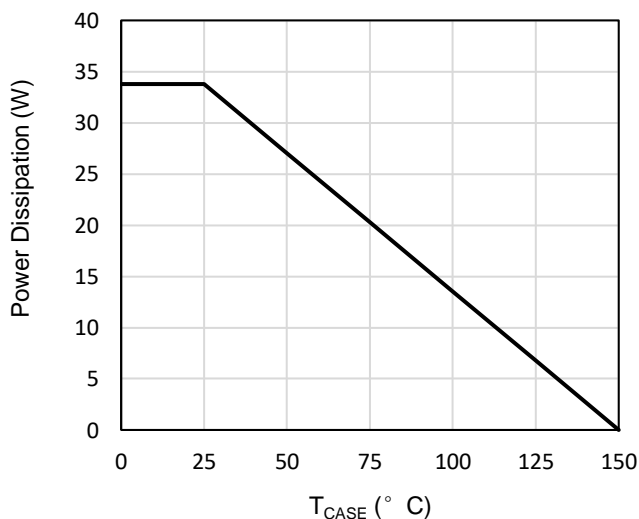


Figure 9: Power De-rating

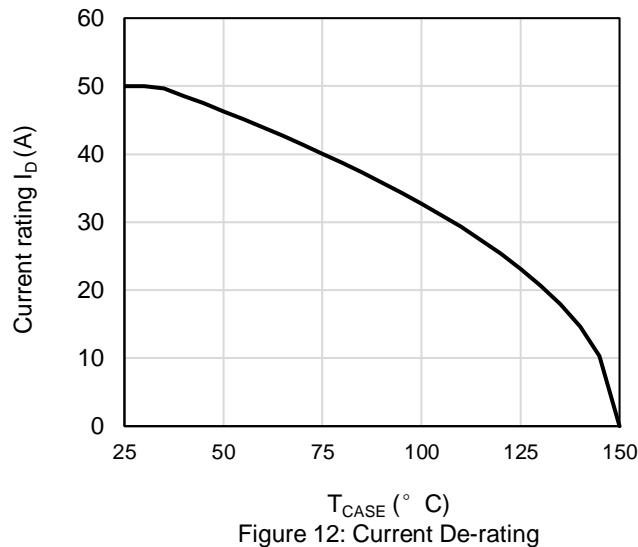


Figure 12: Current De-rating

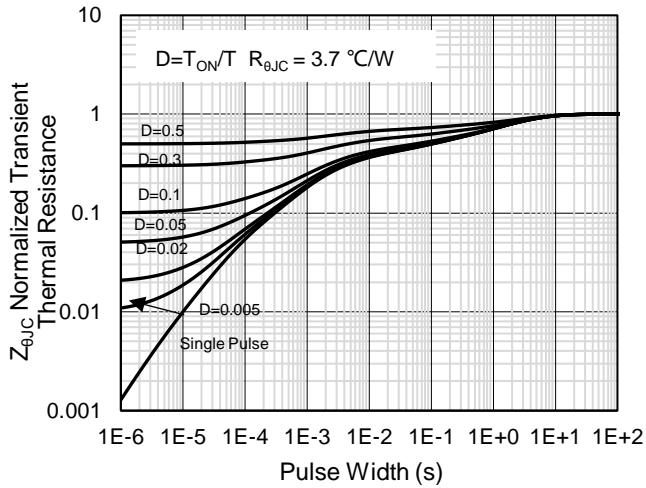


Figure 13: Normalized Maximum Transient Thermal Impedance

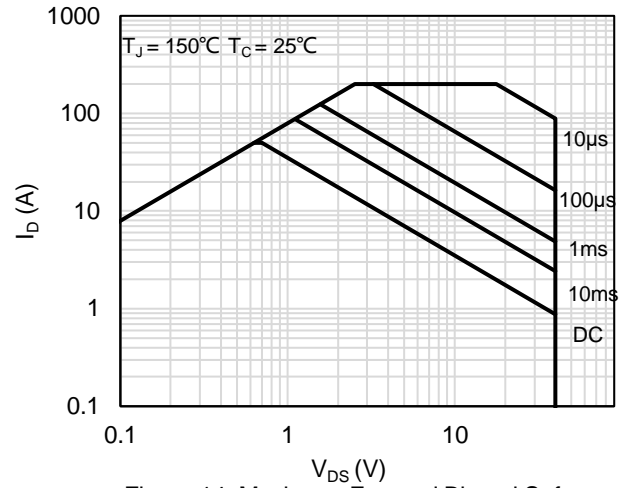
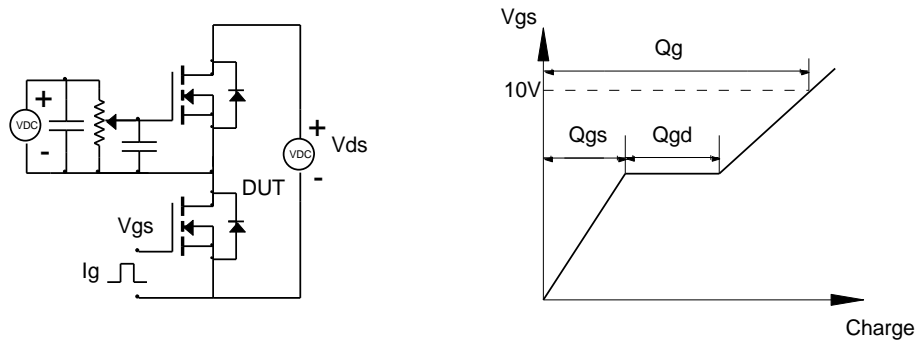


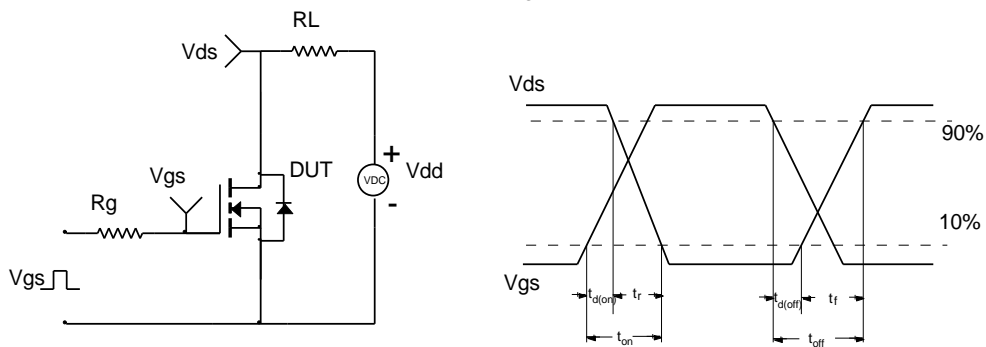
Figure 14: Maximum Forward Biased Safe Operating Area

Test Circuit and Waveform

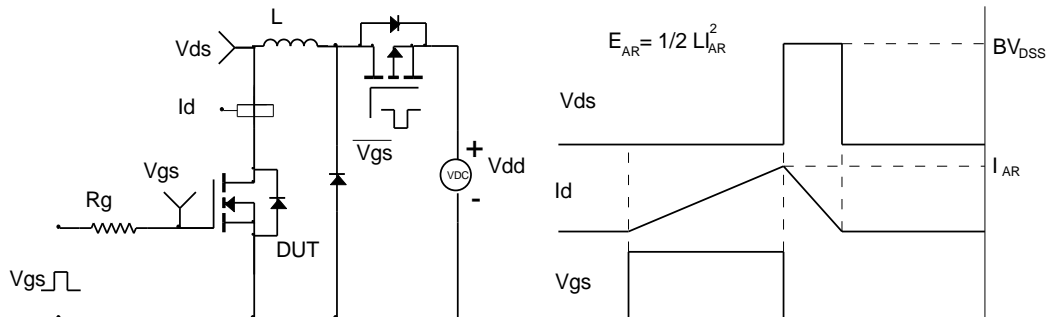
Gate Charge Test Circuit & Waveform



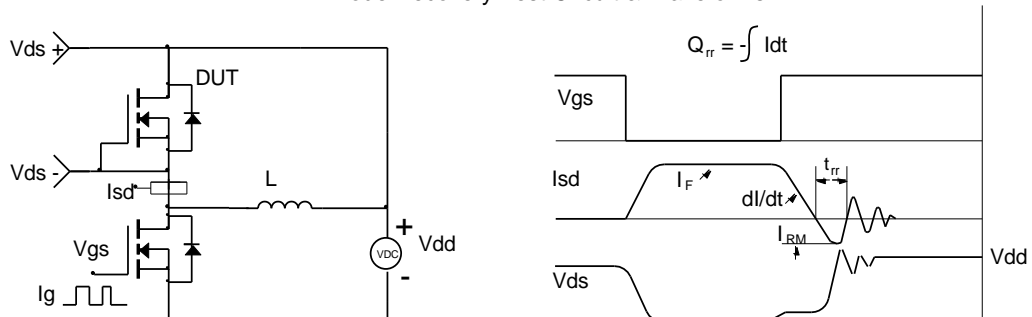
Resistive Switching Test Circuit & Waveforms



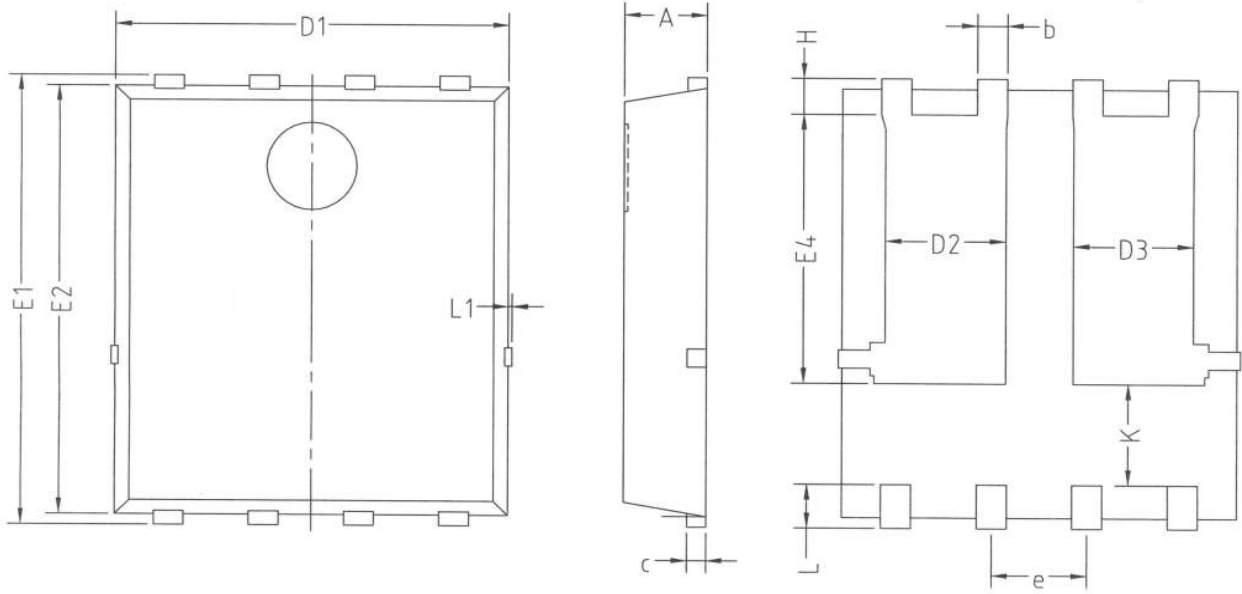
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



DFN5x6-8L Package Information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	1.40	1.60	1.80
D3	1.40	1.60	1.80
e	1.27BSC		
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.47	3.67	3.87
H	0.40	0.50	0.60
K	1.23	1.38	1.53
L	0.30	0.60	0.70
L1			0.12

Customer Service

Sales and Service:

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