

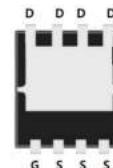


## Features

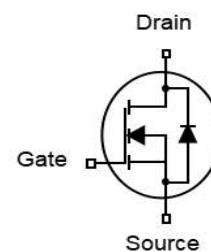
- N-Channel
- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Halogen Free
- 100% EAS Tested

$V_{DS}$	40	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	3.8	$\text{m}\Omega$
$R_{DS(on),TYP}@ V_{GS}=4.5\text{ V}$	5.8	$\text{m}\Omega$
$I_D$	60	A

DFN3x3



Part ID	Package Type	Marking	Packing
ZTG038N04Q	DFN3x3	ZTG038N04Q	5000pcs/Reel



## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit	
<b>Common Ratings (<math>T_c=25^\circ\text{C}</math> Unless Otherwise Noted)</b>				
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	V	
$T_J$	Maximum Junction Temperature	150	$^\circ\text{C}$	
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
$I_{DM}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	$T_c = 25^\circ\text{C}$	240	A
<b>Mounted on Large Heat Sink</b>				
$I_D$	Drain Current-Continuous	$T_c = 25^\circ\text{C}$	60	A
		$T_c = 70^\circ\text{C}$	39	A
$P_D$	Maximum Power Dissipation (Note 3)	$T_c = 25^\circ\text{C}$	40	W
		$T_c = 70^\circ\text{C}$	30	W
<b>Drain-Source Avalanche Ratings</b>				
EAS	Avalanche Energy, Single Pulsed (Note 2)	85	mJ	



**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Electrical Characteristics @ <math>T_J=25^\circ\text{C}</math> (unless otherwise stated)</b>						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	--	--	V
Idss	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}, V_{GS}=0\text{V}$	--	--	1	$\mu\text{A}$
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.5	2.5	V
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=10\text{V}, I_D=10\text{A}$	--	3.8	4.9	$\text{m}\Omega$
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=4.5\text{V}, I_D=8\text{A}$	--	5.8	7.5	$\text{m}\Omega$
<b>Dynamic Electrical Characteristics @ <math>T_J = 25^\circ\text{C}</math> (unless otherwise stated)</b>						
Ciss	Input Capacitance	$V_{DS}=20\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	--	892	--	pF
Coss	Output Capacitance		--	553	--	pF
Crss	Reverse Transfer Capacitance		--	30	--	pF
Rg	Gate resistance	f=1MHz		3.5		$\Omega$
Qg	Total Gate Charge	$V_{DS}=20\text{V}, I_D=50\text{A}, V_{GS}=10\text{V}$	--	16.5	--	nC
Qgs	Gate-Source Charge		--	4.3	--	nC
Qgd	Gate-Drain Charge		--	2.1	--	nC
<b>Switching Characteristics</b>						
Td(on)	Turn-on Delay Time	$V_{DD}=20\text{V}, I_A=50\text{A}, R_G=3\Omega, V_{GS}=10\text{V}$	--	6.3	--	ns
Tr	Turn-on Rise Time		--	2.5	--	ns
Td(off)	Turn-Off Delay Time		--	25	--	ns
Tf	Turn-Off Fall Time		--	3.5	--	ns
<b>Source- Drain Diode Characteristics@ <math>T_J = 25^\circ\text{C}</math> (unless otherwise stated)</b>						
IS	Diode Forward Current		--	--	60	A
VSD	Forward on voltage (Note 3)	$I_S=1\text{A}, V_{GS}=0\text{V}$	--	--	1.2	V
Trr	Reverse Recovery Time	$T_J=25^\circ\text{C}, I_F=50\text{A}$ $dI/dt=100\text{A}/\mu\text{s}$	--	40	--	ns
Qrr	Reverse Recovery Charge		--	22	--	nC

**Notes:**

1.Repetitive rating; pulse width limited by max. junction temperature.

2. $T_J=25^\circ\text{C}, V_G=10\text{V}, R_G=25\Omega, L=0.5\text{ mH}$

3. $P_d$  is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

## Electrical Characteristics Diagrams

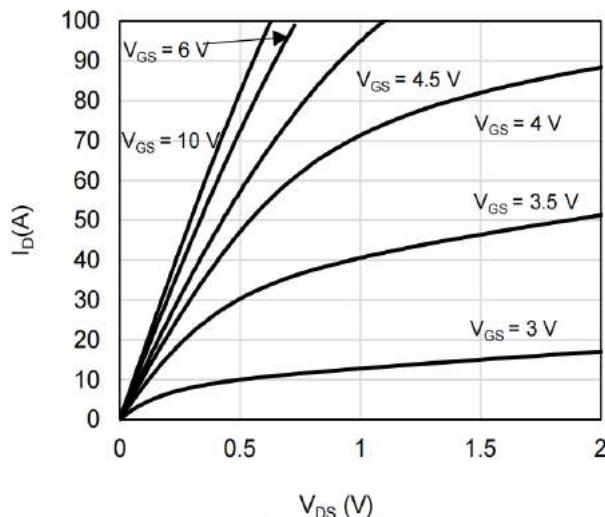


Figure 1: On-Region Characteristics

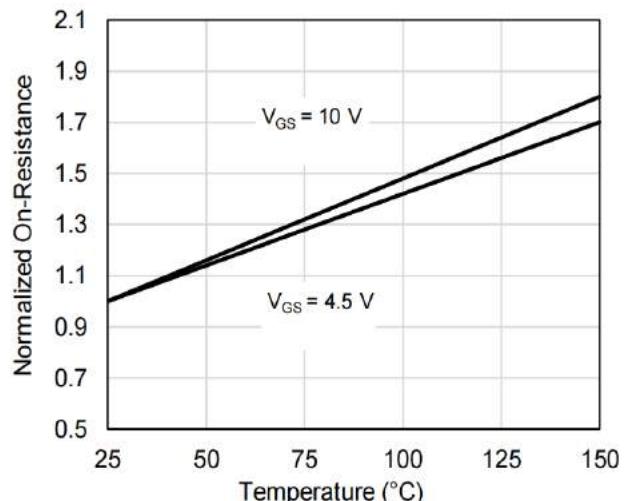


Figure 4: On-Resistance vs. Junction Temperature

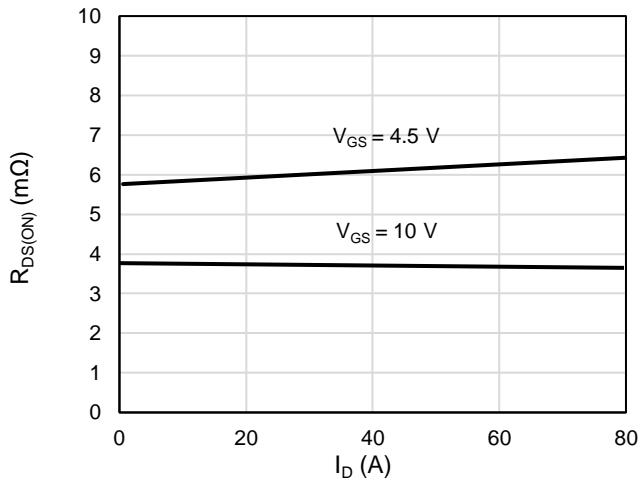


Figure 2: On-Resistance vs. Drain Current and Gate Voltage

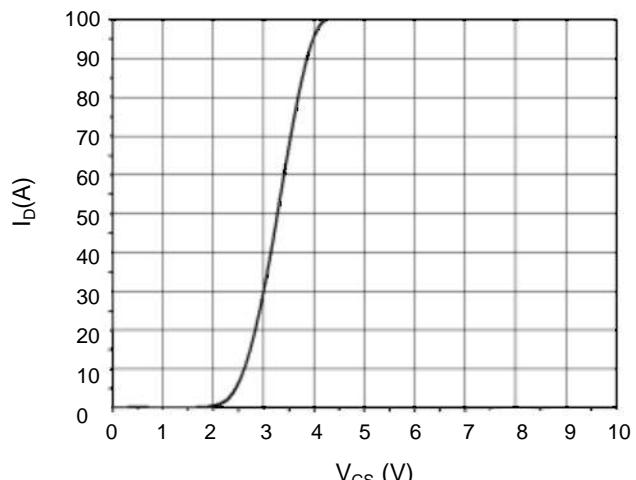


Figure 5: Transfer Characteristics

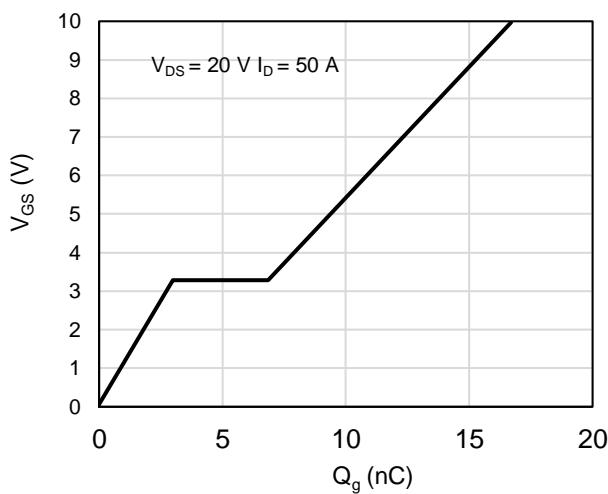


Figure 3: Gate-Charge Characteristics

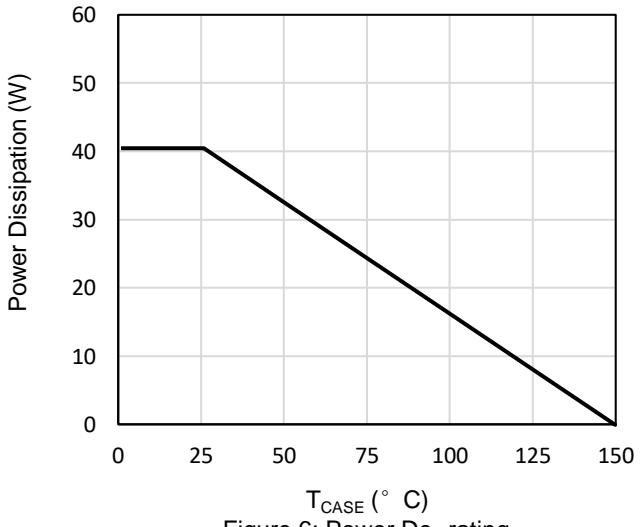


Figure 6: Power De-rating

## Electrical Characteristics Diagrams

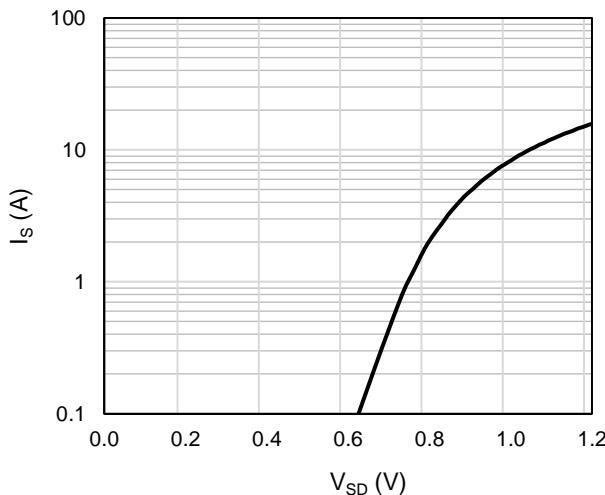


Figure 7: Body-Diode Characteristics

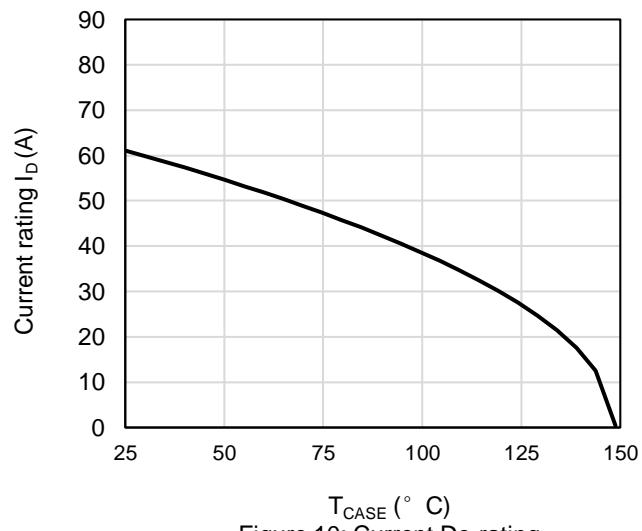


Figure 10: Current De-rating

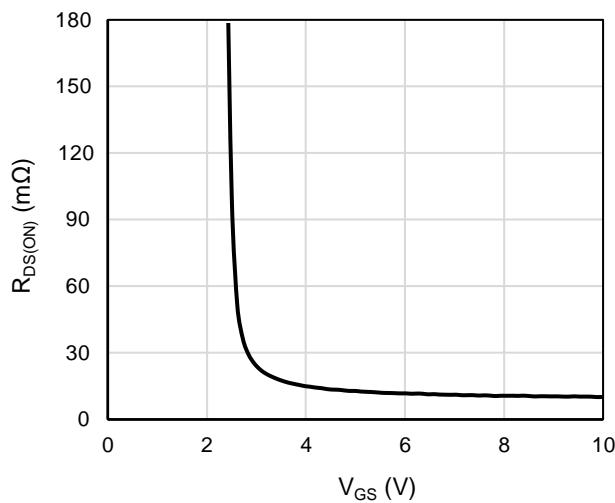


Figure 8: On-Resistance vs. Gate-Source Voltage

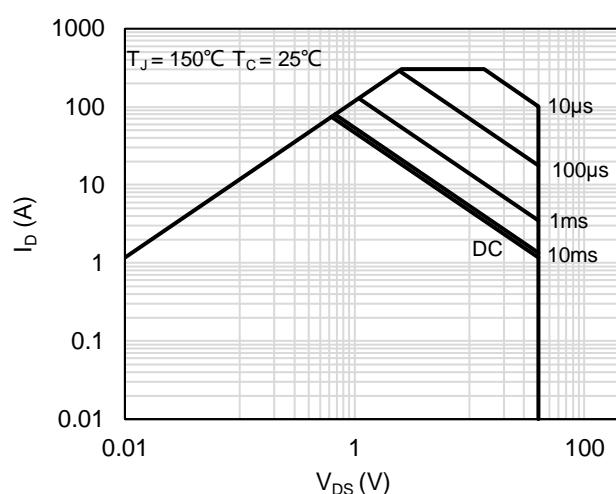


Figure 11: Maximum Forward Biased Safe Operating Area

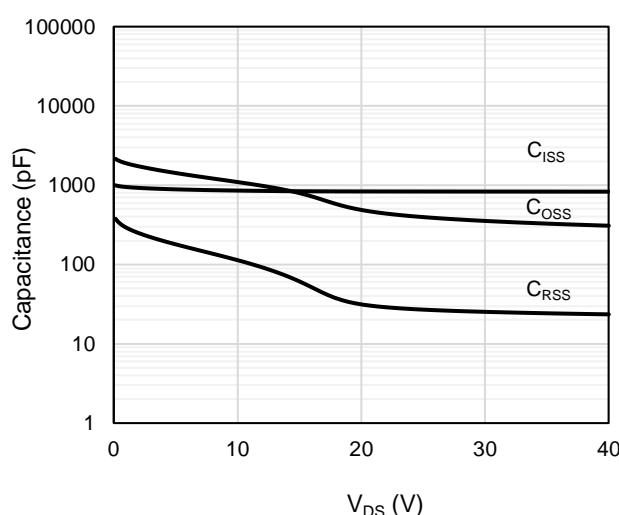


Figure 9: Capacitance Characteristics

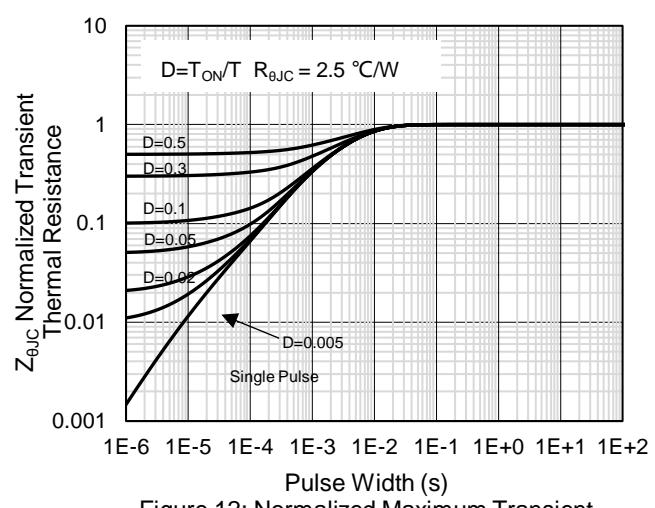
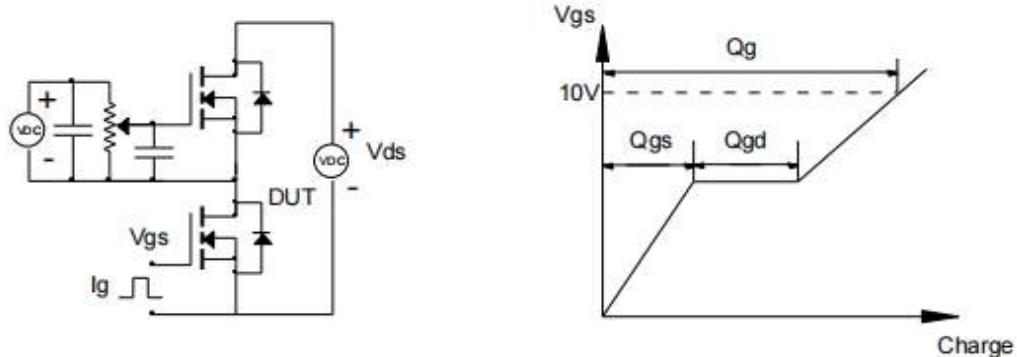


Figure 12: Normalized Maximum Transient Thermal Impedance

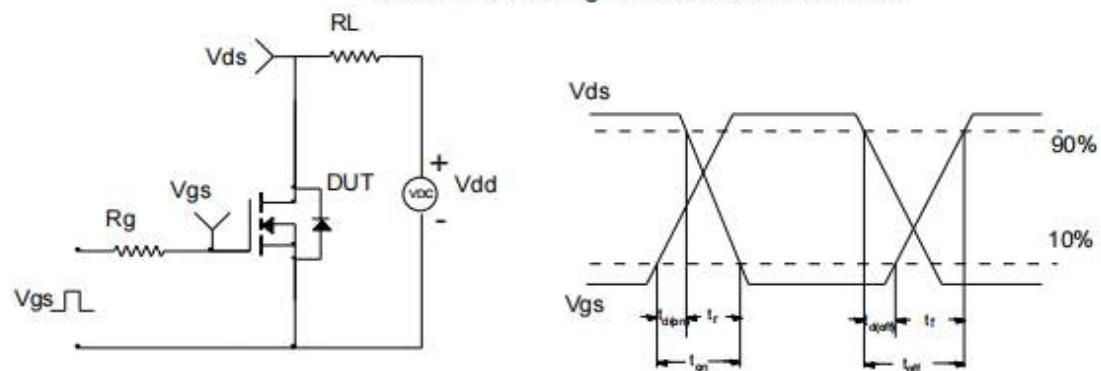


## Test Circuit and Waveform

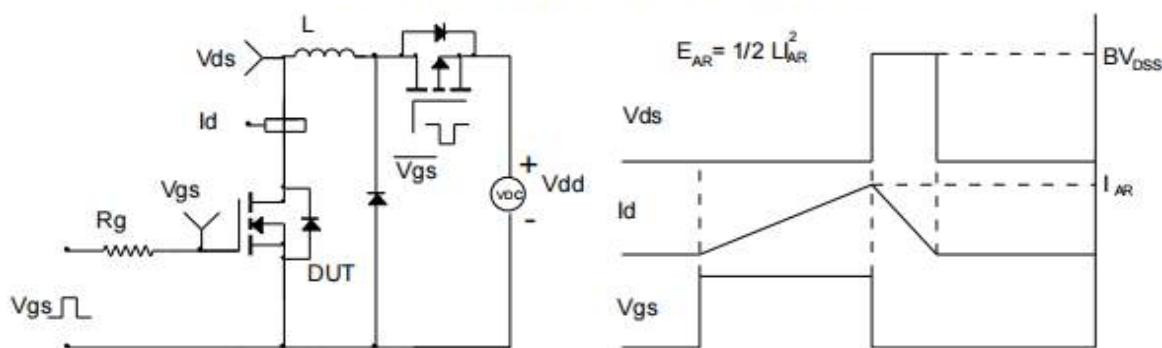
Gate Charge Test Circuit & Waveform



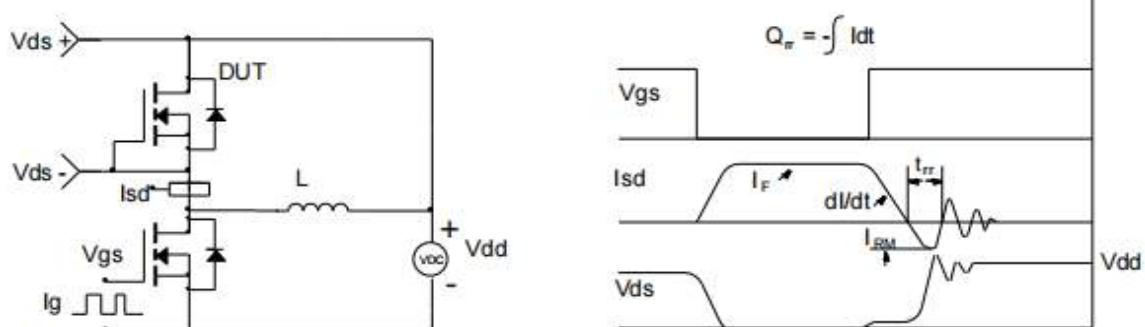
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

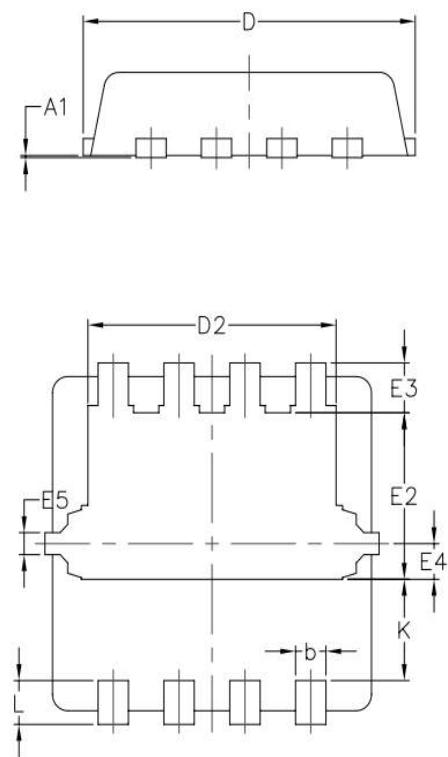
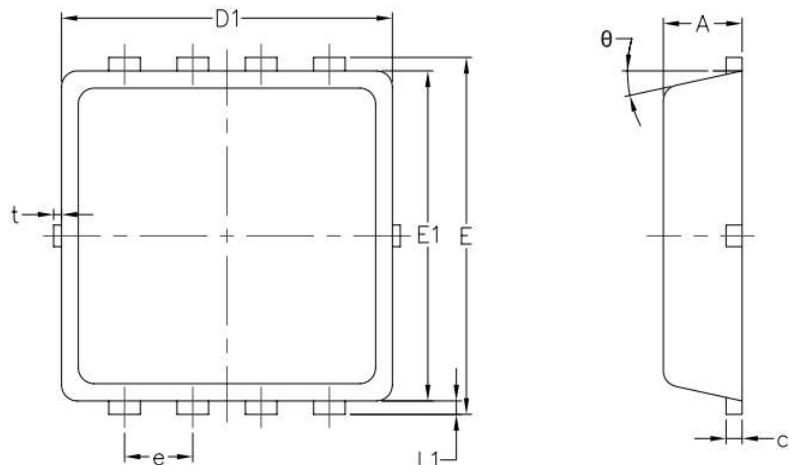


Diode Recovery Test Circuit & Waveforms





## DFN3x3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.32	1.52	1.72
E3	0.28	0.46	0.65
E4	0.18	0.33	0.48
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.78	0.93	1.13
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°

## Customer Service

### Sales and Service:

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