

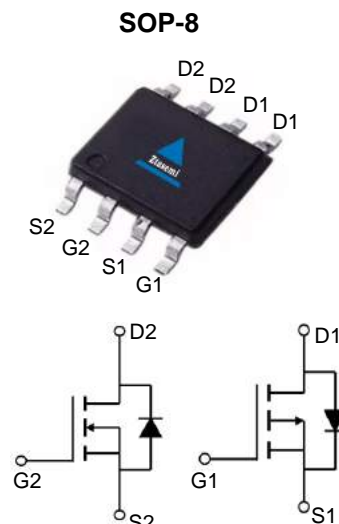
Features

- N and P-Channel
- Advanced Trench Technology
- Super Low Gate Charge
- High Density Cell Design for Ultra Low Rdson
- RoHS Product
- 100% EAS Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	12	m Ω
$R_{DS(on),TYP@ V_{GS}=4.5V}$	16	m Ω
I_D	8	A



Part ID	Package Type	Marking	Packing
ZT4614	SOP-8	ZT4614	4000pcs/reel



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	N-Ch	P-Ch	Unit	
Common Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)					
V_{GS}	Gate-Source Voltage	± 20	± 20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	40	-40	V	
T_J	Maximum Junction Temperature	150	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$	
I_{DM}	Drain Current-Continuous@ Current-Pulsed (Note 1)	$T_C = 25^\circ\text{C}$	32	-32	A
Mounted on Large Heat Sink					
I_D	Drain Current-Continuous	$T_C = 25^\circ\text{C}$	8	-8	A
		$T_C = 100^\circ\text{C}$	5.1	-5.1	A
P_D	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	2	2	W
		$T_C = 100^\circ\text{C}$	0.8	0.8	W
	Maximum Soldering Temperature	260	260	$^\circ\text{C}$	
$R_{\theta JA}$	Thermal Resistance Junction-Ambient (Note 1)	62.5	62.5	$^\circ\text{C/W}$	
Drain-Source Avalanche Ratings					
EAS	Avalanche Energy, Single Pulsed (Note 3)	6.3	6	mJ	

Electrical Characteristics (T_J=25°C unless otherwise noted) N channel

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.7	2.1	V
R _{DS(on)}	Drain-Source On-State Resistance ^(Note 2)	V _{GS} =10V, I _D =8A	--	12	18	mΩ
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =4A	--	16	23	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	443	--	pF
C _{oss}	Output Capacitance		--	109	--	pF
C _{rss}	Reverse Transfer Capacitance		--	10	--	pF
R _g	Gate Resistance	f=1MHz	--	3	--	Ω
Q _g	Total Gate Charge	V _{DS} =20V, I _D =8A, V _{GS} =10V	--	12.1	--	nC
Q _{gs}	Gate-Source Charge		--	3.2	--	nC
Q _{gd}	Gate-Drain Charge		--	3.1	--	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =3A, R _G =3.0Ω, V _{GS} =10V	--	5.1	--	ns
T _r	Turn-on Rise Time		--	3.1	--	ns
T _{d(off)}	Turn-Off Delay Time		--	14.8	--	ns
T _f	Turn-Off Fall Time		--	2.1	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
I _{SD}	Source-Drain Current (Body Diode) ^(Note 1,5)		--	--	8	A
V _{SD}	Forward on voltage ^(Note 2)	I _S =5.5A, V _{GS} =0V	--	--	1.2	V
T _{rr}	Reverse Recovery Time	T _J =25°C, I _F =6A,	--	18	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	10	--	nC

Note :

- Pulse width limited by maximum junction temperature
- EAS (T_J=25°C): NMOS: V_{DD}=20V, I_{AR}=5A, L=0.5mH, R_G=25Ω/ PMOS: V_{DD}=-20V, I_{AR}=-5A, L=0.5mH, R_G=25Ω
- Device on 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one layer, 7μm thick) copper area for drain connection. PCB is vertical in still air.

NMOS Characteristic Curve

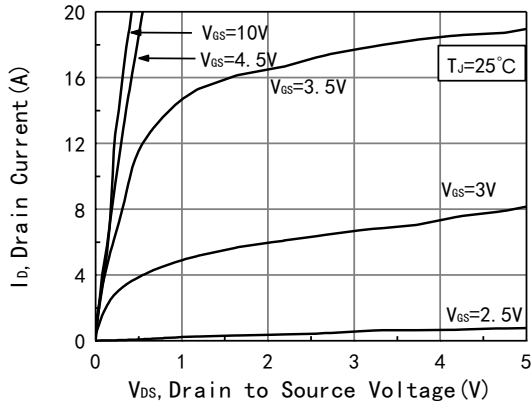


Figure 1. Typical Output Characteristics

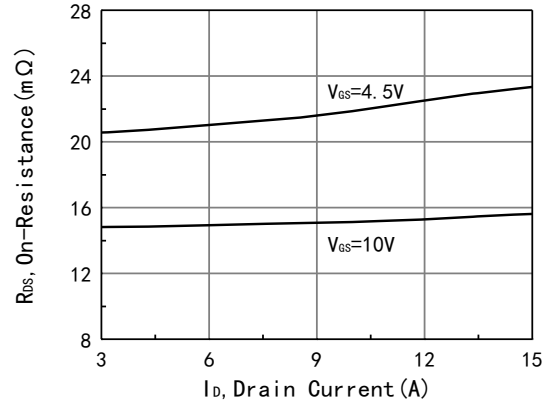


Figure 4. $R_{DS(on)}$ vs. I_D

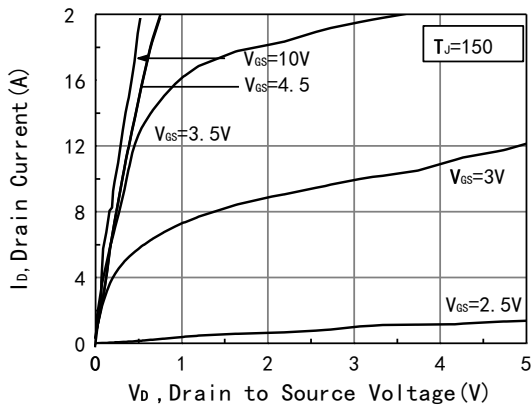


Figure 2. Typical Output Characteristics

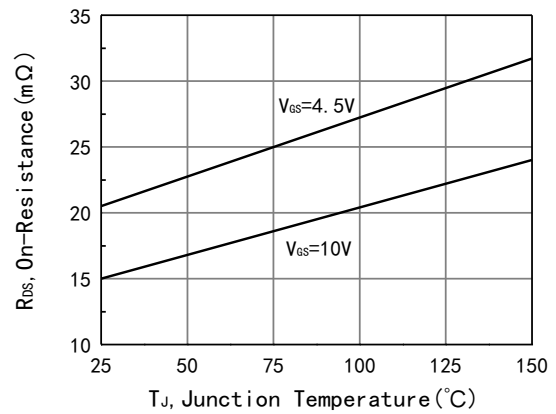


Figure 5. $R_{DS(on)}$ vs. T_J

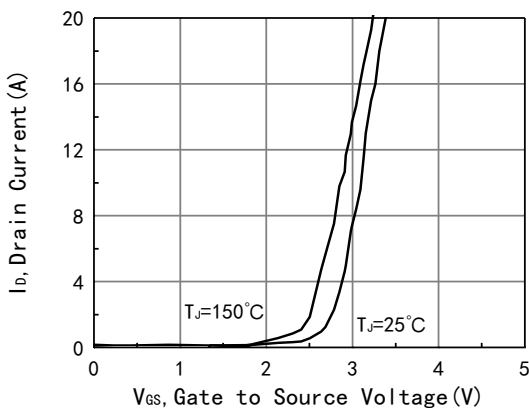


Figure 3. Typical Transfer Characteristics

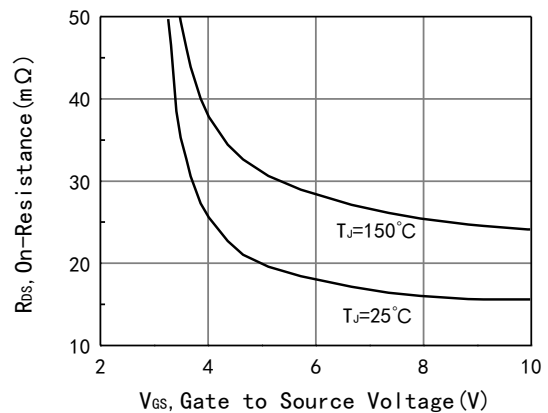


Figure 6. $R_{DS(on)}$ vs. V_{GS}

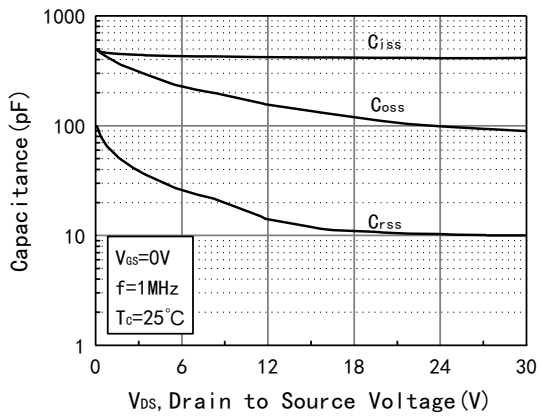


Figure 7. Capacitance vs. V_{ds}

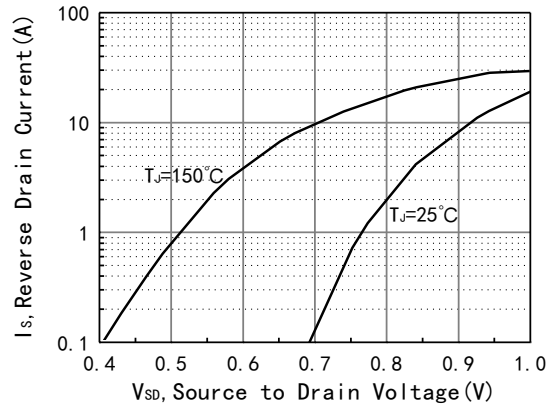


Figure 9. Diode Forward Characteristic

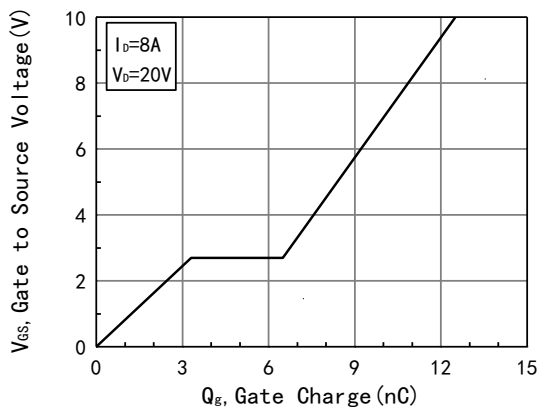


Figure 8. Gate Charge Characteristic

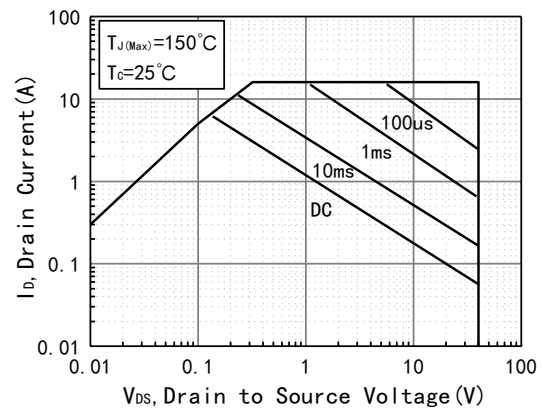


Figure 10. Safe Operating Area

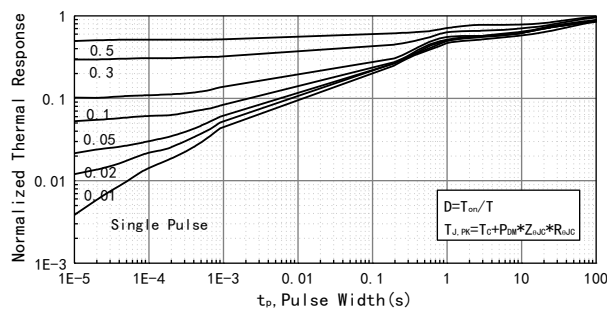


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu s$, Pulse Delay $\leq 200\mu s$.

Electrical Characteristics (T_J=25°C unless otherwise noted) P channel

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V	--	--	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.7	-2.5	V
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-7A	--	29	35	mΩ
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-4.5V, I _D =-4A	--	38	48	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-20V, V _{GS} =0V, f=1MHz	--	548	--	pF
C _{oss}	Output Capacitance		--	107	--	pF
C _{rss}	Reverse Transfer Capacitance		--	57	--	pF
R _g	Gate Resistance	f=1MHz	--	5	--	Ω
Q _g	Total Gate Charge	V _{DS} =-20V, I _D =-8A, V _{GS} =-10V	--	13	--	nC
Q _{gs}	Gate-Source Charge		--	3.9	--	nC
Q _{gd}	Gate-Drain Charge		--	3	--	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =-20V, I _D =-6A, R _G =3.0Ω, V _{GS} =-10V	--	8	--	ns
T _r	Turn-on Rise Time		--	5	--	ns
T _{d(off)}	Turn-Off Delay Time		--	22	--	ns
T _f	Turn-Off Fall Time		--	8.4	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
I _{SD}	Source-Drain Current (Body Diode)		--	--	-8	A
V _{SD}	Forward on voltage (Note 2)	I _S =-5.5A, V _{GS} =0V	--	--	-1.2	V
T _{rr}	Reverse Recovery Time	T _J =25°C, I _F =-5A,	--	21	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	14	--	nC

PMOS Characteristic Curve

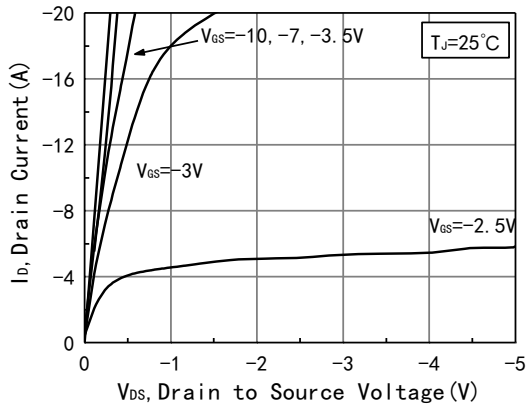


Figure 1. Typical Output Characteristics

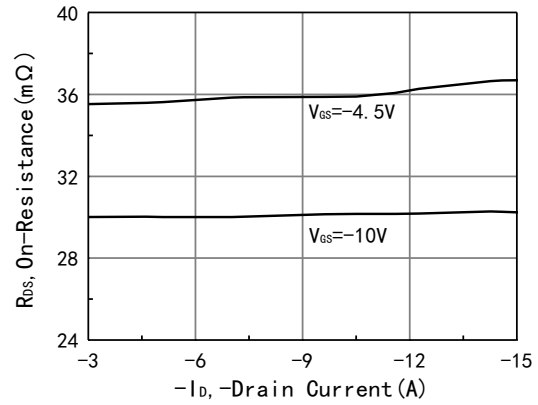


Figure 4. $R_{DS(on)}$ vs. I_D

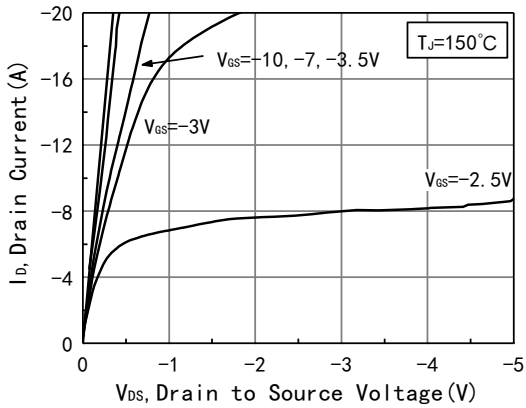


Figure 2. Typical Output Characteristics

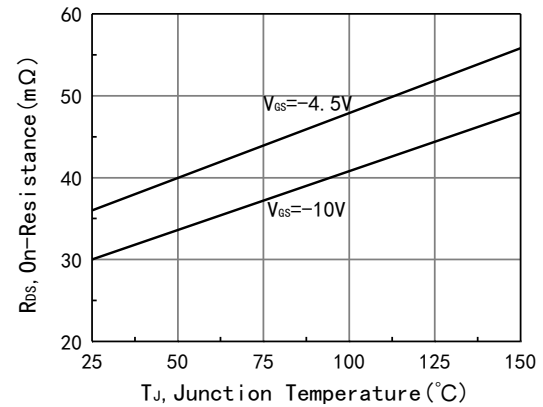


Figure 5. $R_{DS(on)}$ vs. T_J

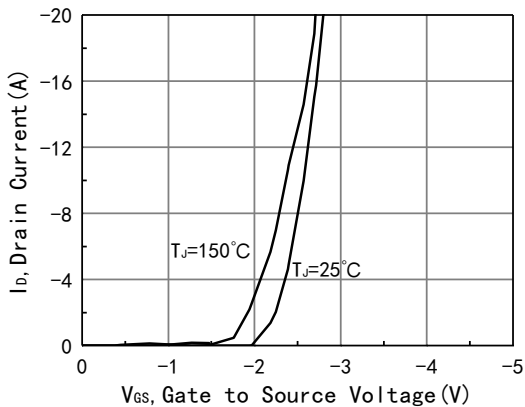


Figure 3. Typical Transfer Characteristics

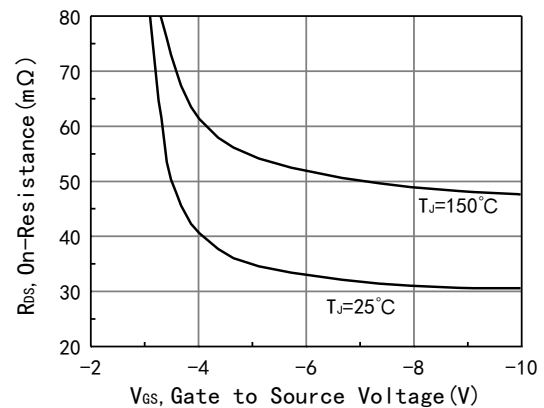


Figure 6. $R_{DS(on)}$ vs. V_{GS}

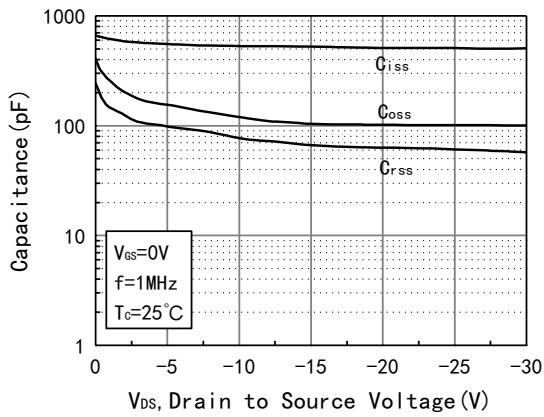


Figure 7. Capacitance vs. V_{ds}

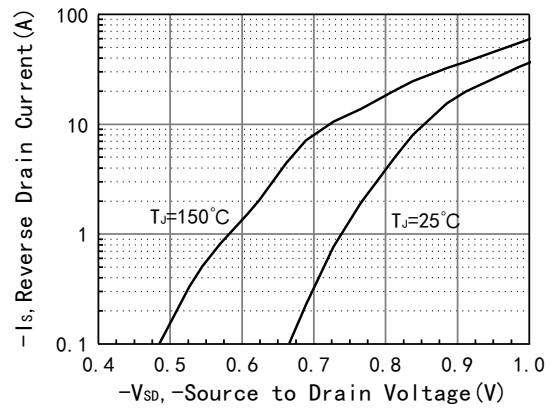


Figure 9. Diode Forward Characteristic

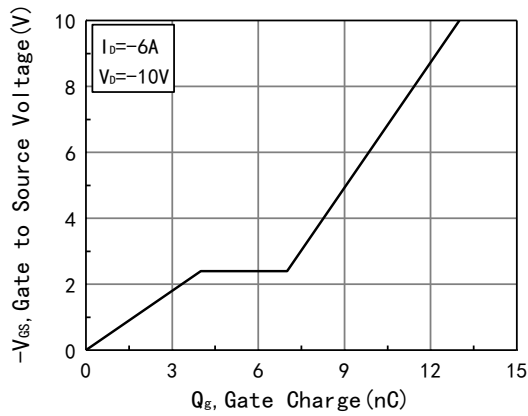


Figure 8. Gate Charge Characteristic

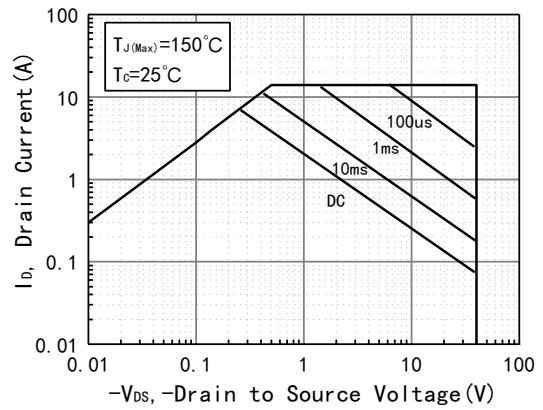


Figure 10. Safe Operating Area

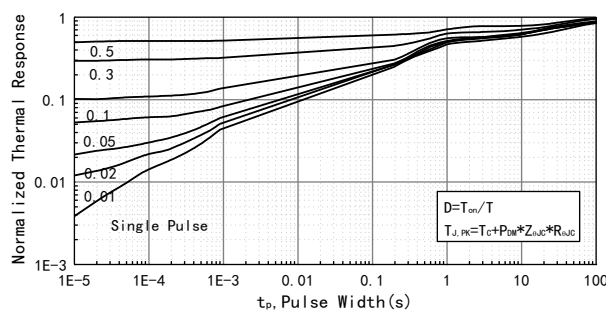
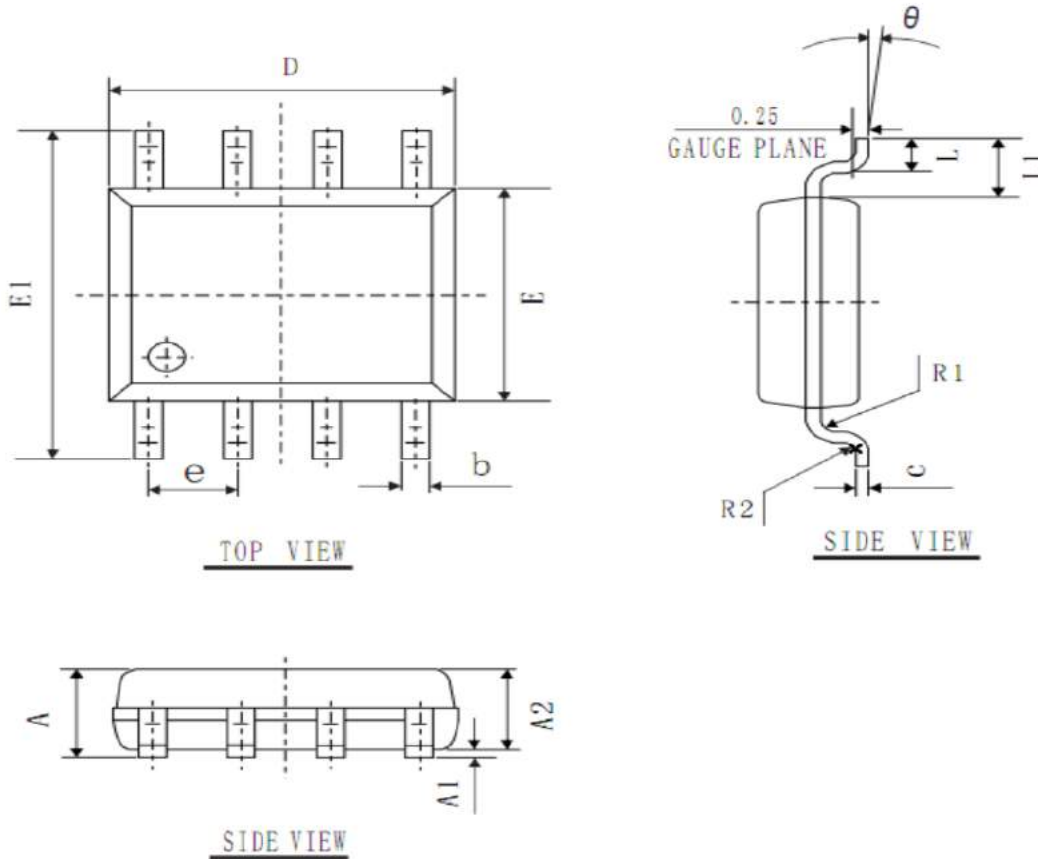


Figure 11. Normalized Maximum Transient Thermal Impedance

Notes:

Pulse Test: Pulse Width $\leq 380\mu s$, Pulse Delay $\leq 200\mu s$.

SOP-8 Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		

Customer Service

Sales and Service:

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