

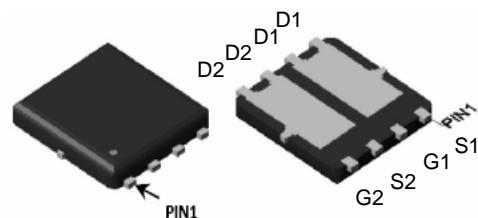


Features

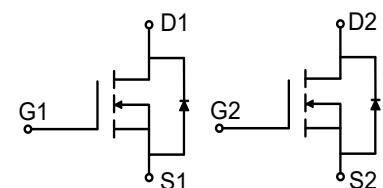
- Dual N-Channel
- Good stability and uniformity
- 100% avalanche tested
- Excellent package for good heat dissipation
- 100% EAS Tested

V_{DS}	30	V
$R_{DS(on),TYP}$ @ $V_{GS}=10$ V	9.3	$\text{m}\Omega$
$R_{DS(on),TYP}$ @ $V_{GS}=4.5$ V	15	$\text{m}\Omega$
I_D	22	A

DFN3x3



Part ID	Package Type	Marking	Packing
ZT10D03Q	DFN3x3	ZT10D03Q	5000pcs/Reel



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
Common Ratings (Tc=25°C Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage	± 20	V	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	30	V	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
I_{DM}	Drain Current-Continuous@ Current-Pulsed (Note 1)	$T_c = 25^\circ\text{C}$	80	A
Mounted on Large Heat Sink				
I_D	Drain Current-Continuous	$T_c = 25^\circ\text{C}$	22	A
		$T_c = 100^\circ\text{C}$	14	A
P_D	Maximum Power Dissipation	40	W	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.2	$^\circ\text{C}/\text{W}$	
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	48	$^\circ\text{C}/\text{W}$	
Drain-Source Avalanche Ratings				
EAS	Avalanche Energy, Single Pulsed (Note 2)	25	mJ	



Electrical Characteristics ($T_j=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	30	--	--	V
Idss	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.5	2.0	V
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=10\text{V}, I_D=15\text{A}$	--	9.3	13	$\text{m}\Omega$
RDS(on)	Drain-Source On-State Resistance	$V_{GS}=4.5\text{V}, I_D=10\text{A}$	--	15	21	$\text{m}\Omega$
gFS	Forward Transconductance	$V_{DS}=5\text{V}, I_D=15\text{A}$	10	--	--	S

Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated) (Note 3,4)

Ciss	Input Capacitance	$V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	--	810	--	pF
Coss	Output Capacitance		--	110	--	pF
Crss	Reverse Transfer Capacitance		--	93	--	pF
Rg	Gate Resistance	f=1MHz	--	2.6	--	Ω
Qg	Total Gate Charge	$V_{DS}=15\text{V}, I_D=10\text{A}, V_{GS}=10\text{V}$	--	14	--	nC
Qgs	Gate-Source Charge		--	4	--	nC
Qgd	Gate-Drain Charge		--	3.5	--	nC

Switching Characteristics (Note 3,4)

Td(on)	Turn-on Delay Time	$V_{DS}=15\text{V}, I_D = 15\text{A}, R_G=3.0\Omega, V_{GS}=10\text{V}$	--	5.1	--	ns
Tr	Turn-on Rise Time		--	4.1	--	ns
Td(off)	Turn-Off Delay Time		--	20.2	--	ns
Tf	Turn-Off Fall Time		--	6.4	--	ns

Source-Drain Diode Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

Is	Diode Forward Current		--	--	22	A
VSD	Forward on voltage	$I_S=22\text{A}, V_{GS}=0\text{V}$	--	--	1.2	V
Trr	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_F = 10\text{A}$ $di/dt=100\text{A}/\mu\text{s}$	--	5.6	--	ns
Qrr	Reverse Recovery Charge		--	5.1	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.5 mH, VDD = 15V, VGS=10V, RG = 25 Ω , Starting Tj = 25°C
3. Isd \leq IMax, di/dt = 100A/us, VDD \leq BVdss, Starting Tj = 25°C
4. Pulse Test : Pulse width \leq 300us, Duty cycle \leq 2%
5. Essentially independent of operating temperature



Typical Characteristics

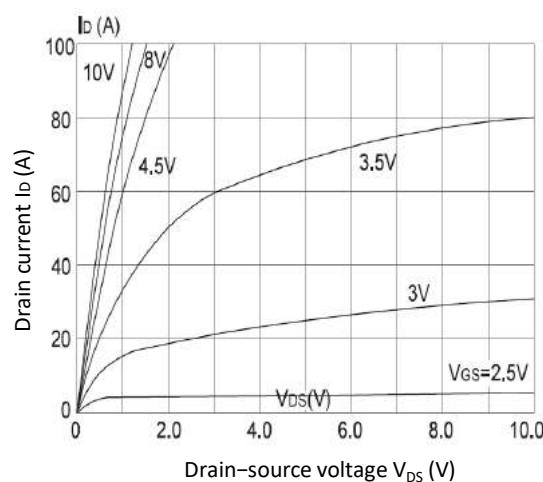


Figure 1. Output Characteristics

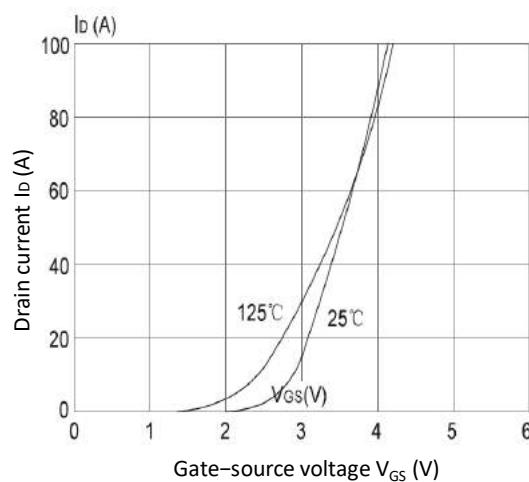


Figure 2. Transfer Characteristics

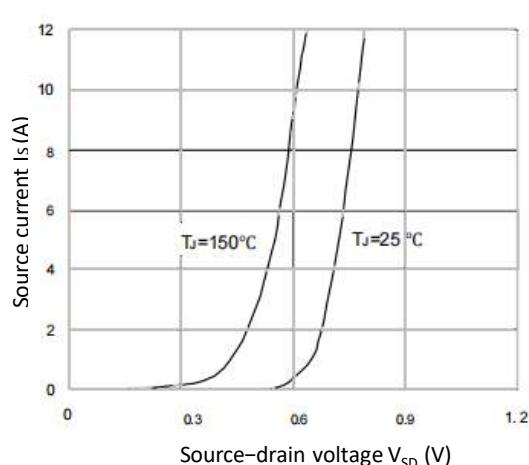


Figure 3. Forward Characteristics of Reverse

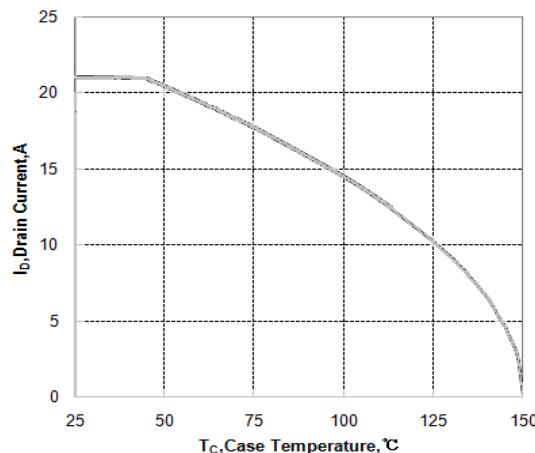


Fig.4 Maximum Continuous Drain Current VS. Case Temperature

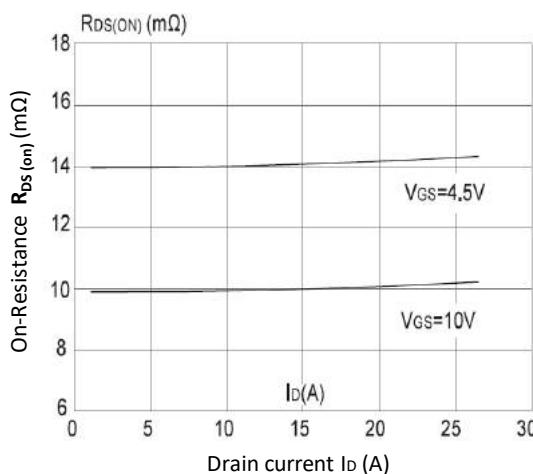


Figure 5. $R_{DS(on)}$ vs. I_D

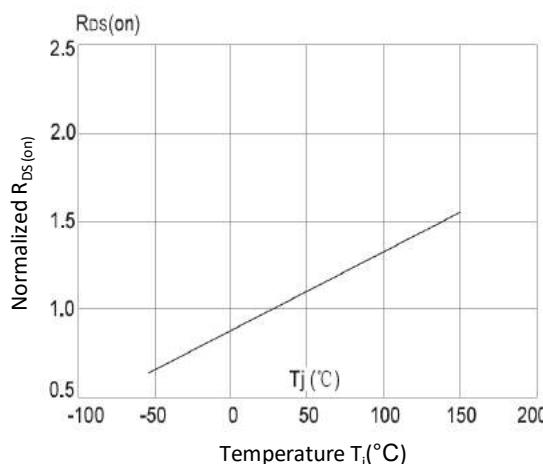


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

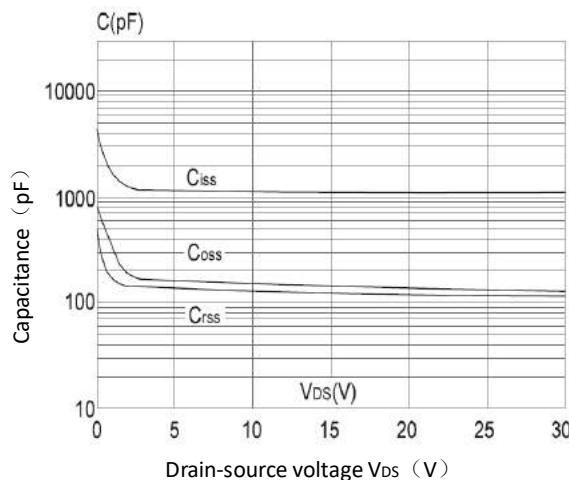


Figure 7. Capacitance Characteristics

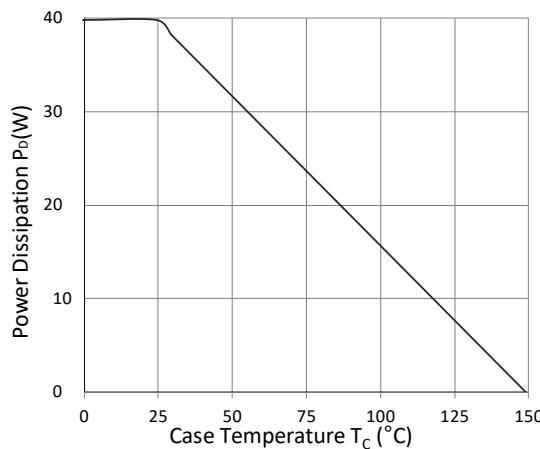


Figure 9. Power Dissipation

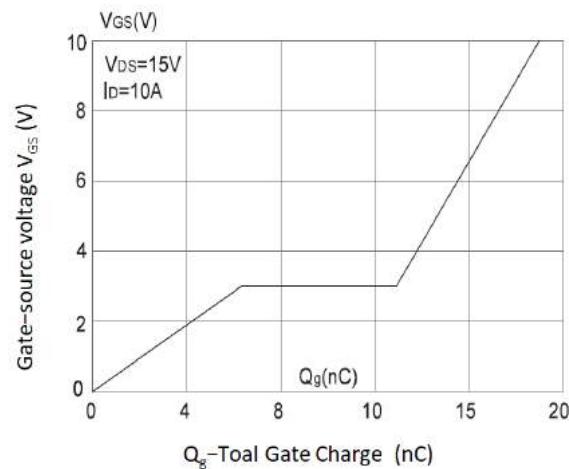


Figure 8. Gate Charge Characteristics

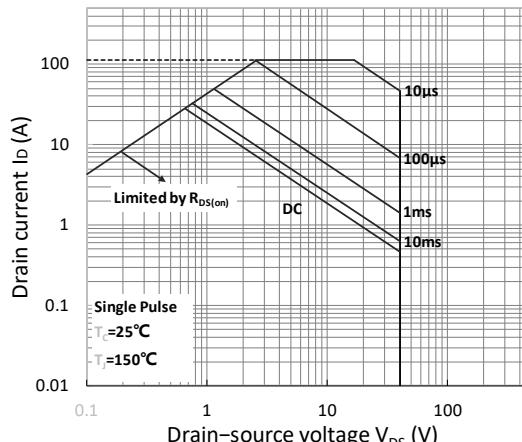


Figure 10. Safe Operating Area

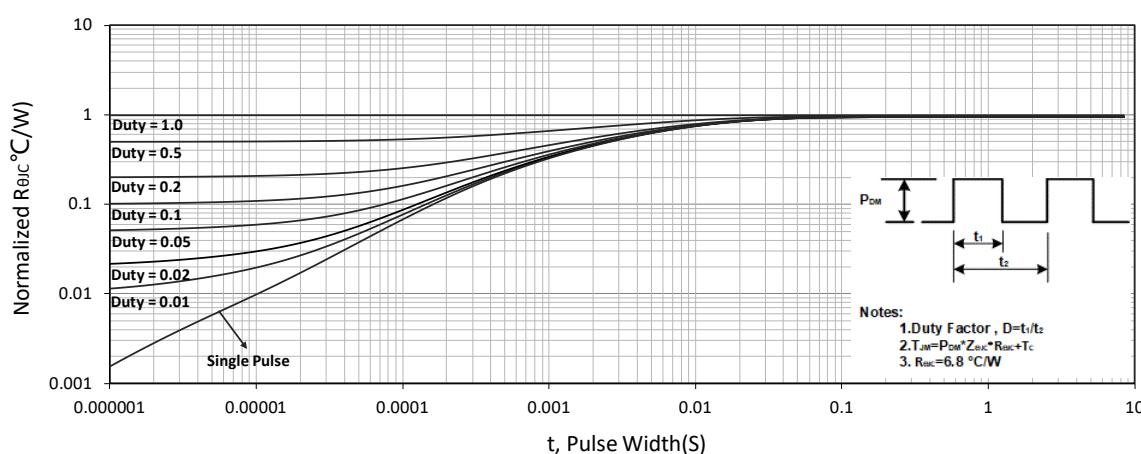


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

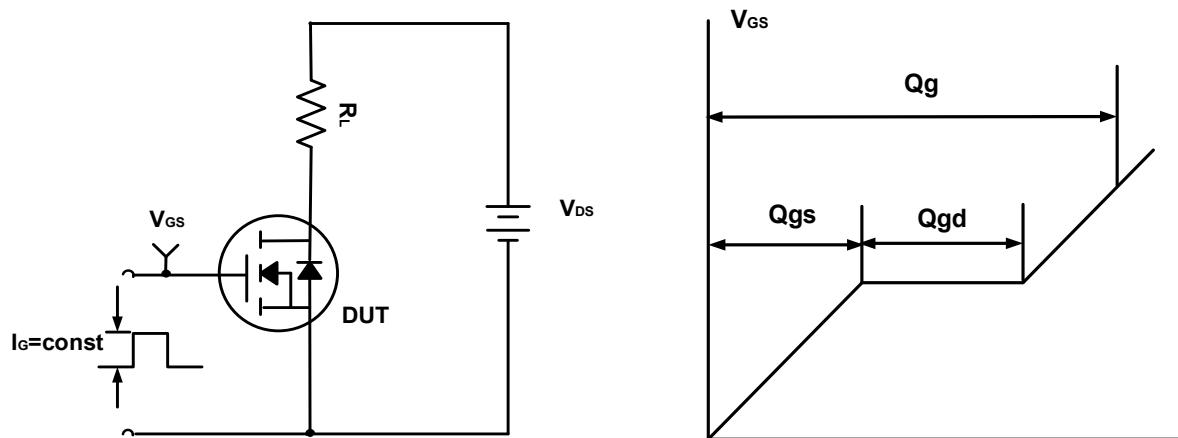


Figure A. Gate Charge Test Circuit & Waveforms

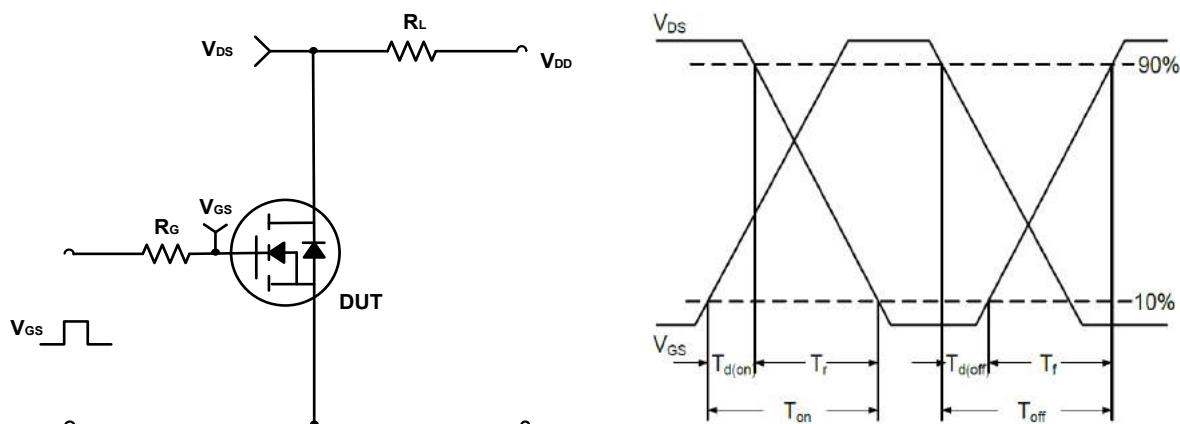


Figure B. Switching Test Circuit & Waveforms

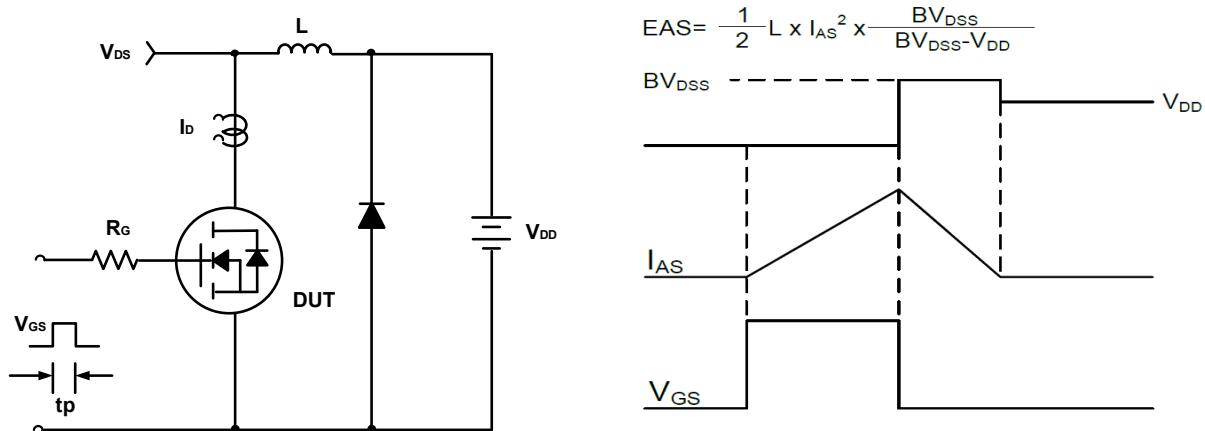
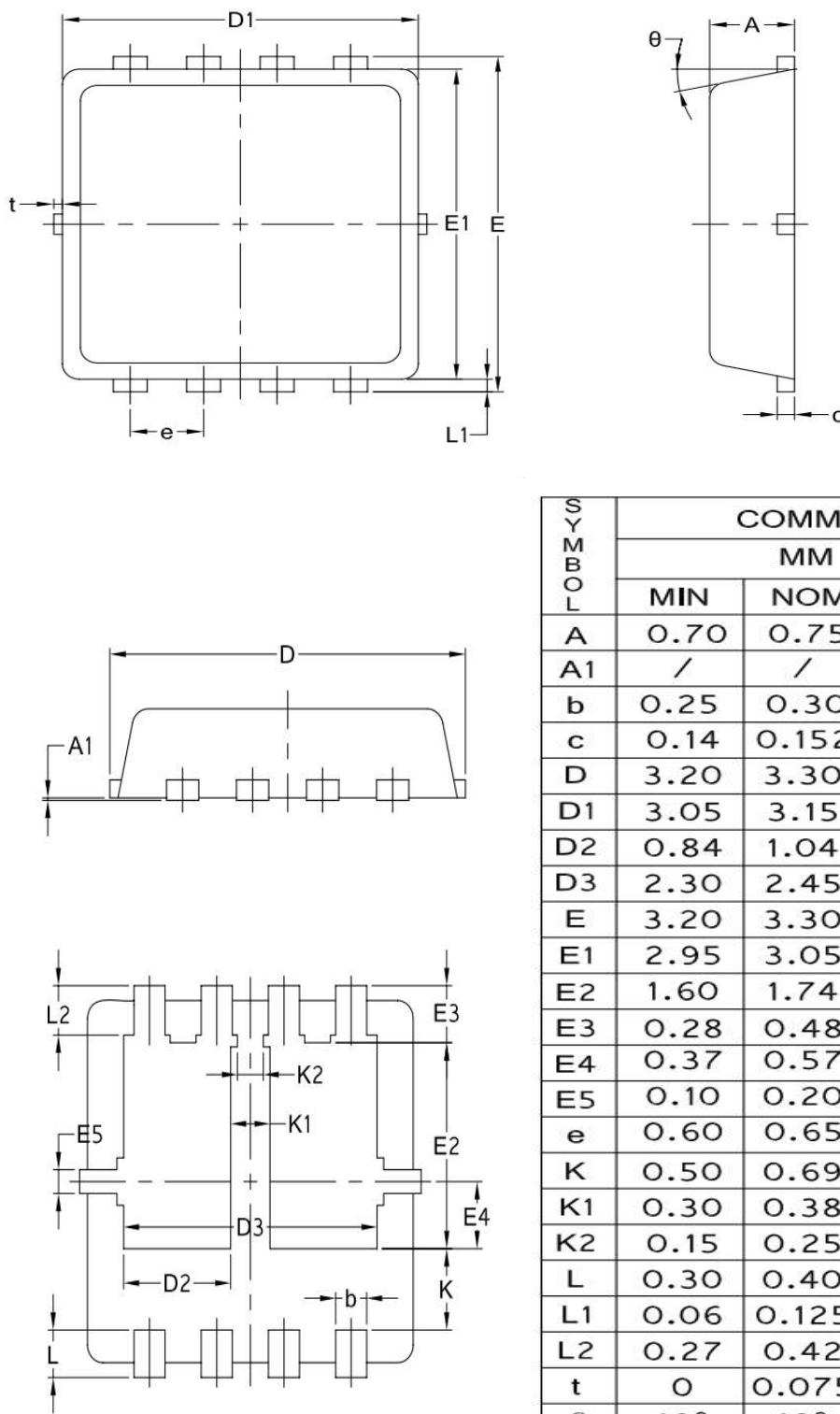


Figure C. Unclamped Inductive Switching Circuit & Waveforms



DFN3x3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
θ	10°	12°	14°

Customer Service

Sales and Service:

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